MIC2800

Digital Power Management IC
2MHz, 600mA DC/DC w/Dual 300mA/300mA Low V_{IN} LDOs

General Description

The MIC2800 is a high performance power management IC, giving three output voltages with maximum efficiency. Integrating a 2MHz DC/DC converter with an LDO post regulator, the MIC2800 gives two high efficiency outputs with a second, 300mA LDO for maximum flexibility. The MIC2800 features a LOWQ® mode, reducing the total current draw while in this mode to less than 30µA. In LOWQ® mode, the output noise of the DC to DC converter is 75µV_{RMS}, significantly lower than other converters which use a PFM light load mode that can interfere with sensitive RF circuitry.

The DC to DC converter uses small values of L and C to reduce board space but still retains efficiencies over 90% at load currents up to 600mA.

The MIC2800 is a µCap design, operating with very small ceramic output capacitors and inductors for stability, reducing required board space and component cost and it is available in fixed output voltages in the 16-pin 3mm x 3mm MLF® leadless package.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- 2.7V to 5.5V input voltage range
- 2MHz DC/DC converter and two stand-alone LDOs
  - LDO1: Low input voltage is powered directly from DC/DC converter for highest efficiency
- Integrated power-on reset (OR function for all outputs)
  - Adjustable delay time
- LOWQ® mode
  - 30µA Total I_Q when in LOWQ® mode
- Tiny 16-pin 3mm x 3mm MLF® package

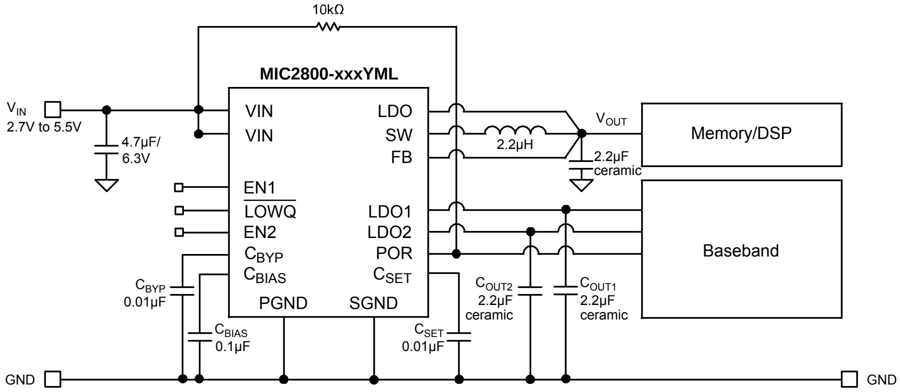
DC to DC Converter
- Output current to 600mA in PWM mode
- LOWQ® Mode: NO NOISE Light load mode
  - 75µV_{RMS} output noise in LOWQ® mode
- 2MHz PWM operation in normal mode
- >90% efficiency

LDOs
- LDO1 input voltage directly connected to DC/DC converter output voltage for maximum efficiency
  - Ideal for 1.8V to 1.5V conversion
  - 300mA output current from 1.8V input
  - Output voltage down to 0.8V
- LDO2 – 300mA output current capable
- Thermal Shutdown Protection
- Current Limit Protection

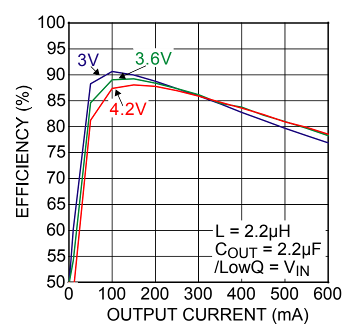
Applications

- Mobile phones
- PDAs
- GPS receivers
- Digital still cameras
- Portable media players

Typical Application



DC/DC 1.8V_{OUT} Efficiency



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MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

Ordering Information

Part number	Manufacturing Part Number	Voltage	Junction Temperature Range	Package
MIC2800-1.8/1.2/2.5YML	MIC2800-G4JYML	1.8V/1.2V/2.5V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-1.8/1.2/2.6YML	MIC2800-G4KYML	1.8V/1.2V/2.6V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-1.8/1.2/2.8YML	MIC2800-G4MYML	1.8V/1.2V/2.8V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-1.8/1.2/3.3YML	MIC2800-G4SYML	1.8V/1.2V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-1.8/1.58/3.3YML	MIC2800-G7SYML	1.8V/1.58V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-1.87/1.2/2.8YML	MIC2800-D24MYML	1.87V/1.2V/2.8V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-1.8/1.5/2.8YML	MIC2800-GFMYML	1.8V/1.5V/2.8V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2800-Adj/1.2/3.3YML	MIC2800-A4SYML	Adj/1.2V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®

Notes:

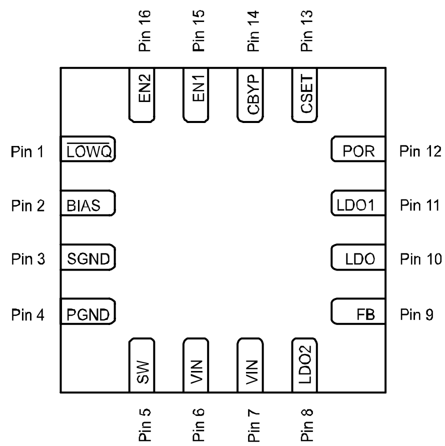
Other voltage options available. Please contact Micrel for details. MLF® is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

DC/DC – Fixed Output Voltages (Range of 1.0V to 2.0V). Adjustable output voltage is available upon request.

LDO1 – Output Voltage Range of 0.8V to $V_{DC/DC}$ - $V_{DO.}$

LDO2 – Output Voltage Range of 0.8V to 3.6V.

Pin Configuration



3mm x 3mm MLF® (ML)
Fixed DC/DC Converter Output Voltage

Pin Description

Pin Number	Pin Name	Pin Function
1	$\overline{\text{LOWQ}}$	LOWQ Mode. Active Low Input. Logic High = Full Power Mode; Logic Low = LOWQ Mode; Do not leave floating.
2	BIAS	Internal circuit bias supply. It must be de-coupled to signal ground with a 0.1µF capacitor and should not be loaded.
3	SGND	Signal ground.
4	PGND	Power ground.
5	SW	Switch (Output): Internal power MOSFET output switches.
6	V_{IN}	Supply Input – DC/DC. Must be tied to PIN7 externally.
7	V_{IN}	Supply Input – LDO2. Must be tied to PIN6 externally.
8	LDO2	Output of regulator 2
9	FB	Feedback. Input to the error amplifier for DC to DC converter. For fixed output voltages connect to V_{OUT} and an internal resistor network sets the output voltage
10	LDO	LDO Output: Connect to V_{OUT} of the DC/DC for LOWQ mode operation.
11	LDO1	Output of regulator 1
12	POR	Power-On Reset Output: Open-drain output. Active low indicates an output undervoltage condition on either one of the three regulated outputs.
13	C_{SET}	Delay Set Input: Connect external capacitor to GND to set the internal delay for the POR output. When left open, there is minimum delay. This pin cannot be grounded.
14	C_{BYP}	Reference Bypass: Connect external 0.1µF to GND to reduce output noise. May be left open.
15	EN1	Enable Input (DC/DC and LDO1). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
16	EN2	Enable Input (LDO 2). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating

Absolute Maximum Ratings(1)

Supply Voltage (V_{IN}) .... 0V to +6V
Enable Input Voltage (V_{EN})................................ 0V to +6V
LOWQ Mode ($V_{\overline{LOWQ}}$). .... 0V to +6V
Power Dissipation, Internally Limited(3)
Lead Temperature (soldering, 10 sec.)..................... 260°C
Storage Temperature (T_s) ....–65°C to +150°C
EDS Rating(4).. 2kV

Operating Ratings(2)

Supply voltage (V_{IN}) .... +2.7V to +5.5V
Enable Input Voltage (V_{EN}).................................. 0V to V_{IN}
LOWQ Mode ($V_{\overline{LOWQ}}$). .... 0V to V_{IN}
Junction Temperature (T_J) ....–40°C to +125°C
Junction Thermal Resistance
MLF-16 (θ_{JA})...45°C/W

Electrical Characteristics(5)

V_{IN} = EN1 = EN2 = $\overline{LOWQ}$ = V_{OUT}(6) + 1V; $C_{OUTDC/DC}$ = 2.2µF, C_{OUT1} = C_{OUT2} = 2.2µF; $I_{OUTDC/DC}$ = 100mA; $I_{OUTLDO1}$ = $I_{OUTLDO2}$ = 100µA; T_J = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
UVLO Threshold	Rising input voltage during turn-on	**2.45**	2.55	**2.65**	V
UVLO Hysteresis			100		mV
Ground Pin Current	V_{FB} = GND (not switching); LDO2 Only (EN1 = LOW)		800 55	1100 85 **95**	µA µA µA
Ground Pin Current in Shutdown	All EN = 0V		0.2	5	µA
Ground Pin Current (LOWQ mode)	$I_{DC/DC}$ ≤ I_{LDO1} ≤ I_{LDO2} ≤ 10mA DC/DC and LDO1 OFF; I_{LDO2} ≤ 10mA		30 20	60 **80** **70**	µA µA µA
Over-temperature Shutdown			160		°C
Over-temperature Shutdown Hysteresis			23		°C
Enable Inputs (EN1; EN2; /LOWQ)					
Enable Input Voltage	Logic Low			**0.2**	V
	Logic High	**1.0**			V
Enable Input Current	V_{IL} ≤ 0.2V		0.1	**1**	µA
	V_{IH} ≥ 1.0V		0.1	**1**	µA
Turn-on Time (See Timing Diagram)					
Turn-on Time (LDO1 and LDO2)	EN2=V_{IN} EN1=V_{IN}		240 120	**500** **350**	µs µs
Turn-on Time (DC/DC)	EN2=V_{IN}; I_{LOAD} = 300mA; C_{BYP} = 0.1µF		83	**350**	µs
POR Output					
VTH	Low Threshold, % of nominal ($V_{DC/DC}$ or V_{LDO1} or V_{LDO2}) (Flag ON)	90	91		%
	High Threshold, % of nominal ($V_{DC/DC}$ AND V_{LDO1} AND V_{LDO2}) (Flag OFF)		96	99	%
VOL	POR Output Logic Low Voltage; IL = 250µA		10	**100**	mV
IPOR	Flag Leakage Current, Flag OFF		0.01	**1**	µA
SET INPUT					
SET Pin Current Source	VSET = 0V	0.75	1.25	1.75	µA
SET Pin Threshold Voltage	POR = High		1.25		V

Electrical Characteristics - DC/DC Converter

$V_{IN} = V_{OUTDC/DC} + 1$; EN1 = V_{IN}; EN2 = GND; $I_{OUTDC/DC}$ = 100mA ;L = 2.2µH; $C_{OUTDC/DC}$ = 2.2µF; T_J = 25°C, **bold** values indicate –40°C to + 125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{LOWQ}}$ = High (Full Power Mode)					
Fixed Output Voltages	Nominal V_{OUT} tolerance	-2 **-3**		+2 **+3**	% %
Current Limit in PWM Mode	$V_{FB} = 0.9*V_{NOM}$	0.75	1	1.6	A
FB pin input current (ADJ only)			1	5	nA
Output Voltage Line Regulation	V_{OUT} > 2.4V; $V_{IN} = V_{OUT}$ + 300mV to 5.5V, I_{LOAD}= 100mA V_{OUT} < 2.4V; V_{IN} = 2.7V to 5.5V, I_{LOAD}= 100mA		0.2		%/V %/V
Output Voltage Load Regulation	20mA < I_{LOAD} < 300mA		0.2	1.5	%
Maximum Duty Cycle	$V_{FB} \leq 0.4V$	100			%
PWM Switch ON-Resistance	I_{SW} = 150mA $V_{FB} = 0.7V_{FB\_NOM}$ I_{SW} = -150mA $V_{FB} = 1.1V_{FB\_NOM}$		0.6 0.8		Ω Ω
Oscillator Frequency		**1.8**	2	**2.2**	MHz
Output Voltage Noise	C_{OUT} = 2.2µF; C_{BYP} = 0.1µF; 10Hz to 100KHz		60		μV_{RMS}
$\overline{\text{LOWQ}}$ = Low (Light Load Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	-2.0		+2.0	%
	Variation from nominal V_{OUT}; -40°C to +125°C	**-3.0**		**+3.0**	%
Output Voltage Temp. Coefficient			40		ppm/C
Line Regulation	$V_{IN} = V_{OUT}$ + 1V to 5.5V; I_{OUT} = 100µA		0.02	0.3 **0.6**	%/V %/V
Load Regulation	I_{OUT} = 100µA to 50mA		0.2	1.5	%
Ripple Rejection	f = up to 1kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF f = 20kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF		55 45		dB dB
Current Limit	V_{OUT} = 0V	80	120	**190**	mA

Electrical Characteristics - LDO1

$V_{IN} = V_{OUTDC/DC}$; EN1 = V_{IN}; EN2 = GND; C_{OUT1} = 2.2µF, I_{OUT1} = 100µA; T_J = 25°C, **bold** values indicate –40°C $\le T_J \le$ +125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{LOWQ}$ = High (Full Power Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	-2.0		+2.0	%
	Variation from nominal V_{OUT}; -40°C to +125°C	**-3.0**		**+3.0**	%
Output Current Capability	$V_{IN} \ge 1.8V$ $V_{IN} \ge 1.5V$	300 120			mA mA
Load Regulation	I_{OUT} = 100µA to 150mA I_{OUT} = 100µA to 300mA		0.17 0.3	1.5	% %
Current Limit	V_{OUT} = 0V	350	500	700	mA
Ripple Rejection	f = up to 1kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF f = 20kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF		70 44		dB dB
Output Voltage Noise	C_{OUT} = 2.2µF; C_{BYP} = 0.1µF; 10Hz to 100KHz		30		μV_{RMS}
$\overline{LOWQ}$ = Low (Light Load Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	-3.0		+3.0	%
	Variation from nominal V_{OUT}; -40°C to +125°C	**-4.0**		**+4.0**	%
Load Regulation	I_{OUT} = 100µA to 10mA		0.2	0.5 **1.0**	% %
Current Limit	V_{OUT} = 0V	50	85	125	mA
Ripple Rejection	f = up to 1kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF f = 20kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF		70 42		dB dB

Electrical Characteristics - LDO2

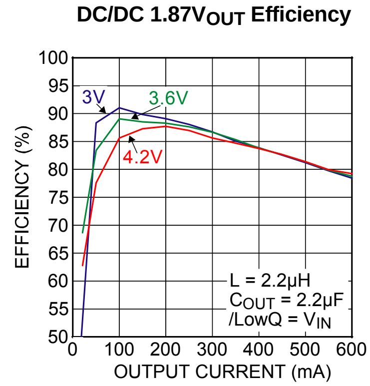
$V_{IN} = V_{OUTLDO2} + 1.0V$; EN1 = GND; EN2 = V_{IN}; $C_{OUT2} = 2.2\mu F$; $I_{OUTLDO2} = 100\mu A$; $T_J = 25°C$, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted.

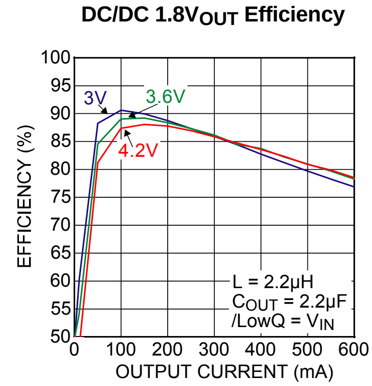
Parameter	Conditions	Min	Typ	Max	Units
$\overline{LOWQ}$ = High (Full Power Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	-2.0		+2.0	%
	Variation from nominal V_{OUT}; -40°C to +125°C	**-3.0**		**+3.0**	%
Line Regulation	$V_{IN} = V_{OUT}$ +1V to 5.5V; $I_{OUT} = 100\mu A$		0.02	0.3 **0.6**	%/V
Load Regulation	$I_{OUT} = 100\mu A$ to 150mA $I_{OUT} = 100\mu A$ to 200mA $I_{OUT} = 100\mu A$ to 300mA		0.20 0.25 0.40	**1.5**	% % %
Dropout Voltage	I_{OUT} = 150mA I_{OUT} = 200mA I_{OUT} = 300mA		70 94 142	**300**	mV mV mV
Ripple Rejection	f = up to 1kHz; $C_{OUT} = 2.2\mu F$; $C_{BYP} = 0.1\mu F$ f = 20kHz; $C_{OUT} = 2.2\mu F$; $C_{BYP} = 0.1\mu F$		75 40		dB dB
Current Limit	V_{OUT} = 0V	400	550	850	mA
Output Voltage Noise	$C_{OUT} = 2.2\mu F$, $C_{BYP} = 0.1\mu F$, 10Hz to 100kHz		25		μV_{RMS}
$\overline{LOWQ}$ = Low (Light Load Mode)					
Output Voltage Accuracy	Variation from nominal V_{OUT}	-3.0		+3.0	%
	Variation from nominal V_{OUT}; -40°C to +125°C	**-4.0**		**+4.0**	%
Line Regulation	$V_{IN} = V_{OUT}$ +1V to 5.5V		0.02	0.3 **0.6**	%/V
Load Regulation	$I_{OUT} = 100\mu A$ to 10mA		0.2	**1.0**	%
Dropout Voltage	I_{OUT} = 10mA		22	35 **50**	mV mV
Ripple Rejection	f = up to 1kHz; $C_{OUT} = 2.2\mu F$; $C_{BYP} = 0.1\mu F$ f = 20kHz; $C_{OUT} = 2.2\mu F$; $C_{BYP} = 0.1\mu F$		75 55		dB dB
Current Limit	V_{IN} = 2.7V; V_{OUT} = 0V	50	85	125	mA

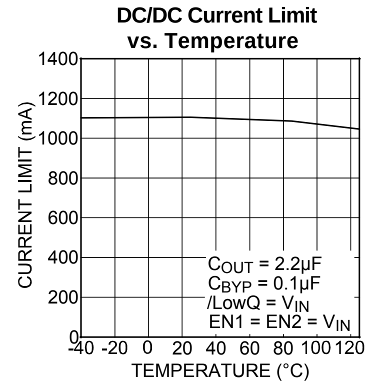
Notes:

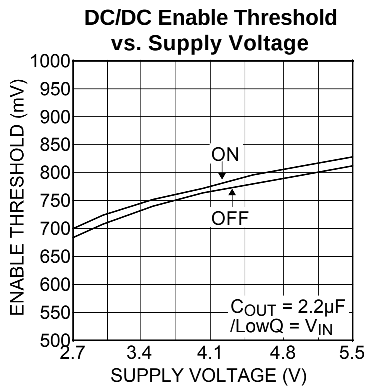
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.
6. V_{OUT} denotes the highest of the three output voltage plus one volt.

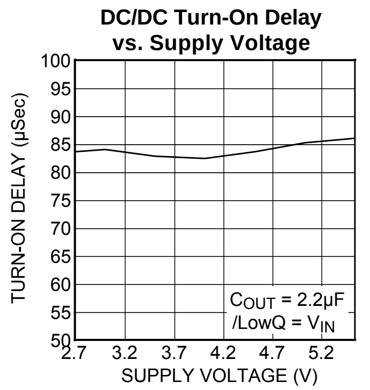
Typical Characteristics (DC/DC PWM Mode)





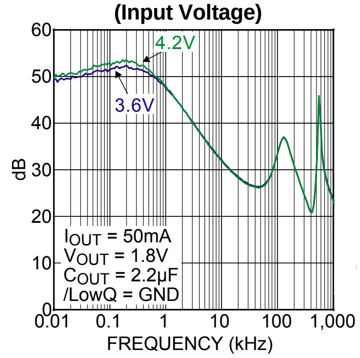




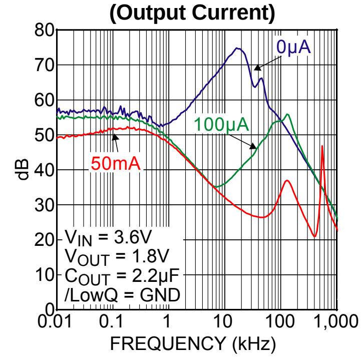


Typical Characteristics (DC/DC LowQ Mode)

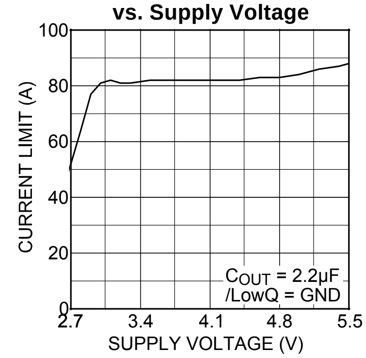
Power Supply Rejection Ratio (Input Voltage)



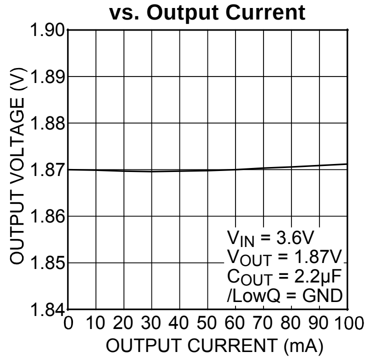
Power Supply Rejection Ratio (Output Current)



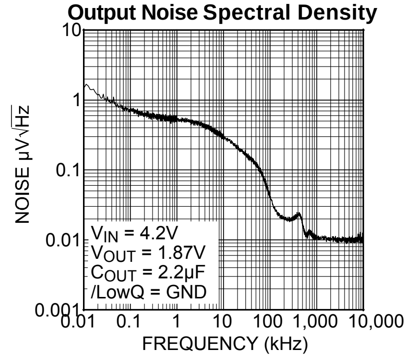
LDO Current Limit vs. Supply Voltage



LDO Output Voltage vs. Output Current

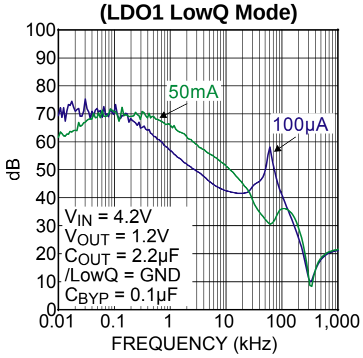


DC/DC LowQ Mode Output Noise Spectral Density

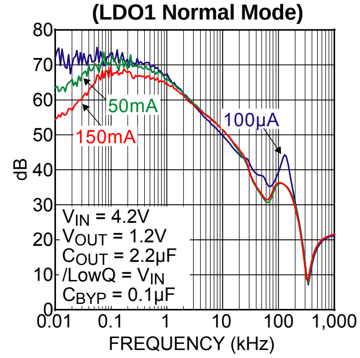


Typical Characteristics (LDO1, LDO2)

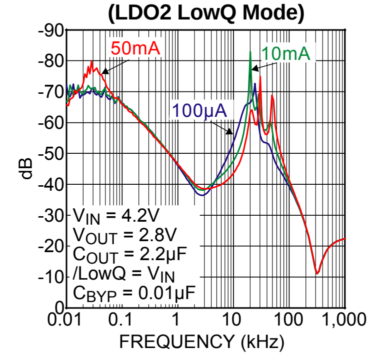
Power Supply Rejection Ratio (LDO1 LowQ Mode)



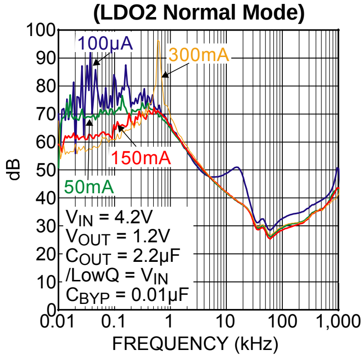
Power Supply Rejection Ratio (LDO1 Normal Mode)



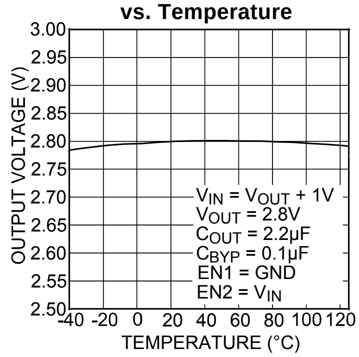
Power Supply Rejection Ratio (LDO2 LowQ Mode)



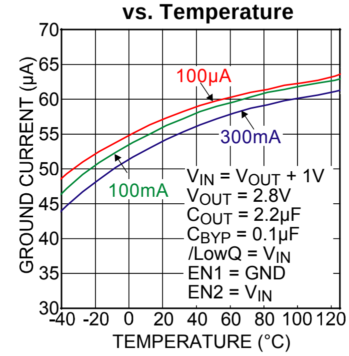
Power Supply Rejection Ratio (LDO2 Normal Mode)



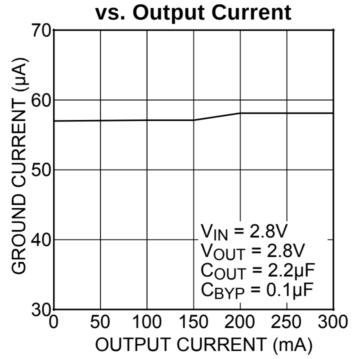
(LDO2) Output Voltage vs. Temperature



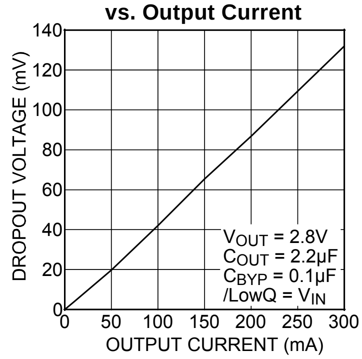
Ground Current vs. Temperature



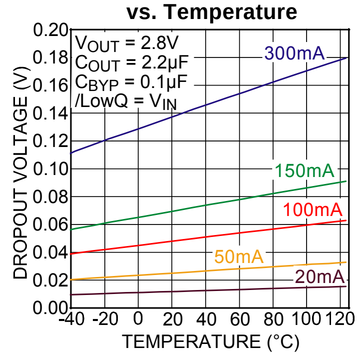
Ground Current vs. Output Current



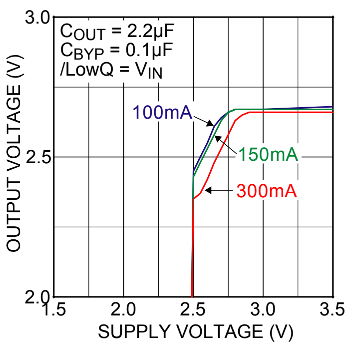
(LDO2) Dropout Voltage vs. Output Current



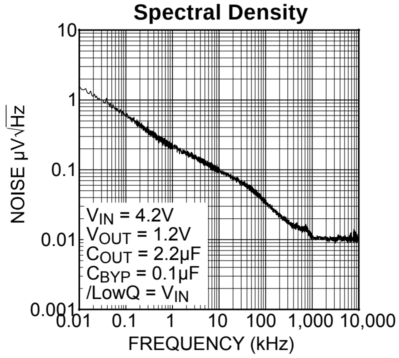
(LDO2) Dropout Voltage vs. Temperature



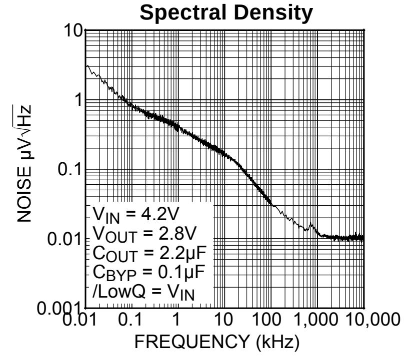
Dropout Charracteristics



LDO1 Output Noise Spectral Density

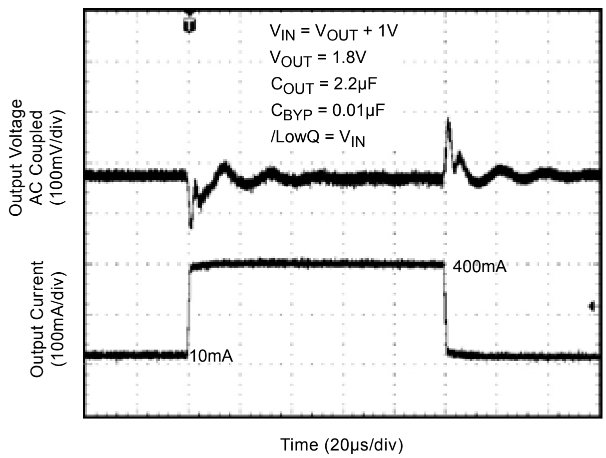


LDO2 Output Noise Spectral Density

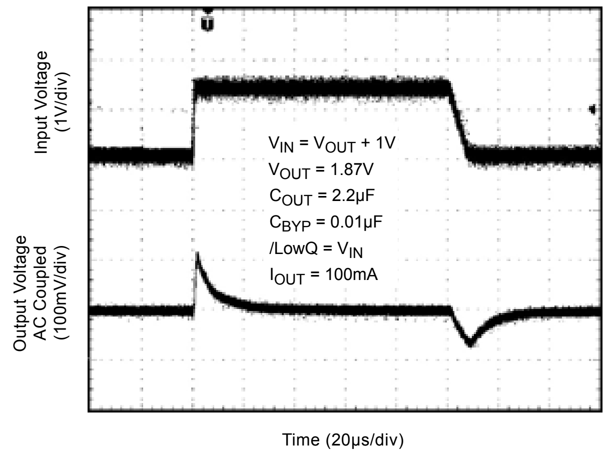


Functional Characteristics

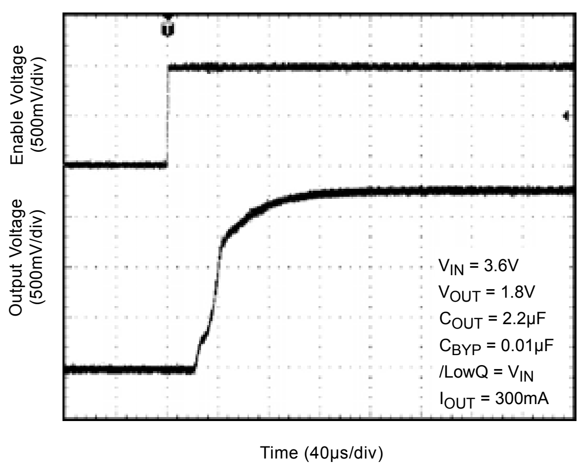
DC/DC Load Transient PWM Mode



DC/DC Line Transient PWM Mode

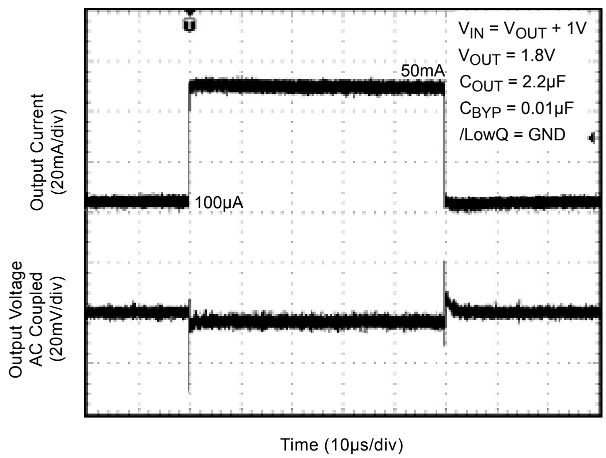


Enable Transient PWM Mode

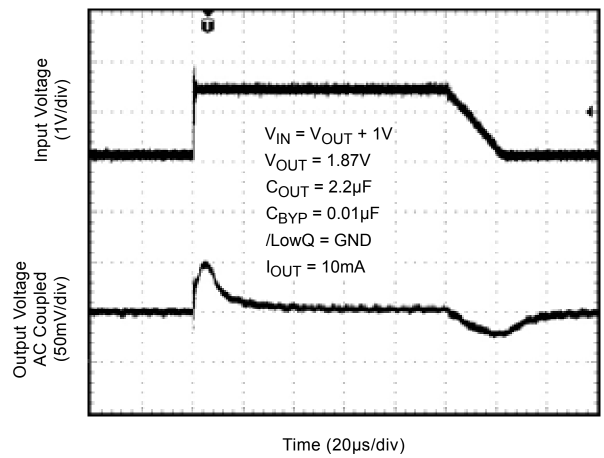


Functional Characteristics

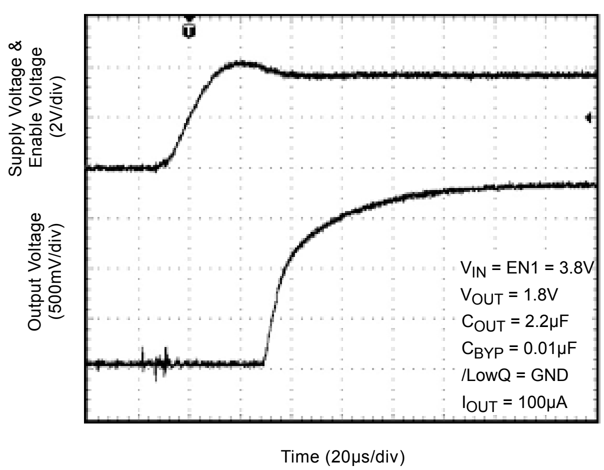
DC/DC Load Transient LowQ Mode



DC/DC Line Transient LowQ Mode

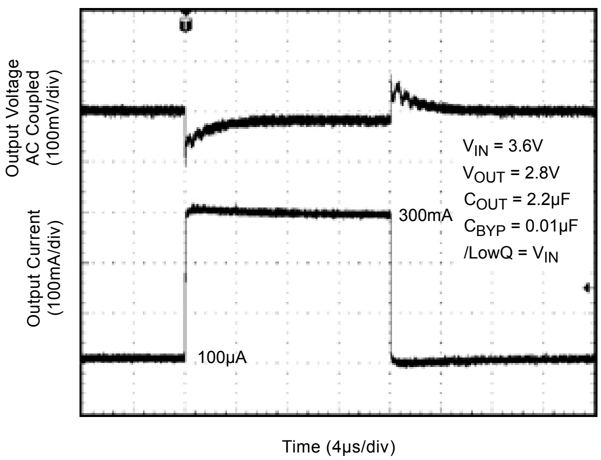


Enable Transient LowQ Mode

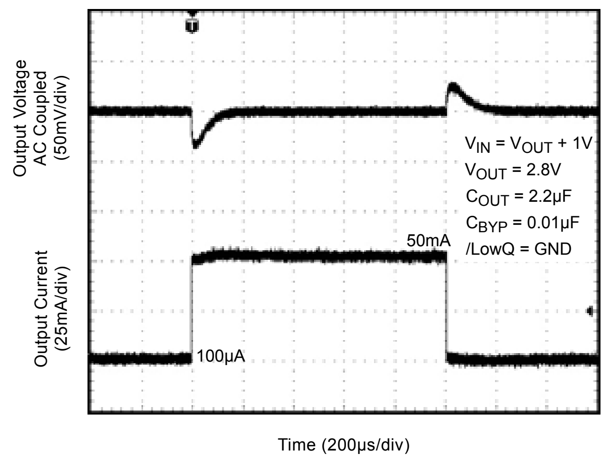


Functional Characteristics

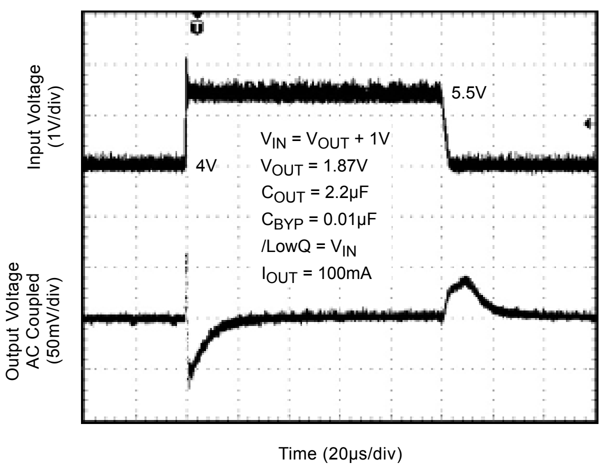
LDO2 Load Transient Normal Mode



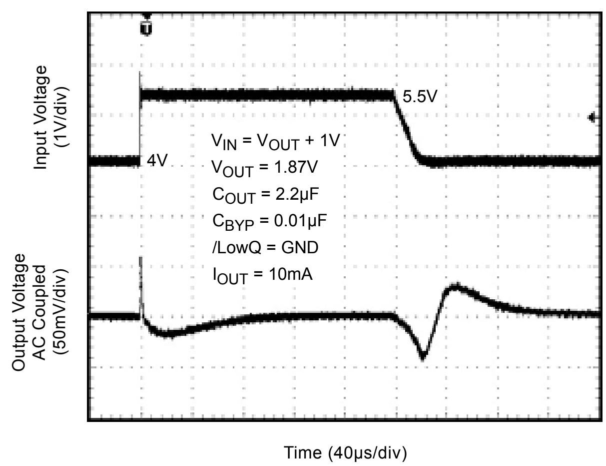
LDO2 Load Transient LowQ Mode



LDO2 Line Transient Normal Mode

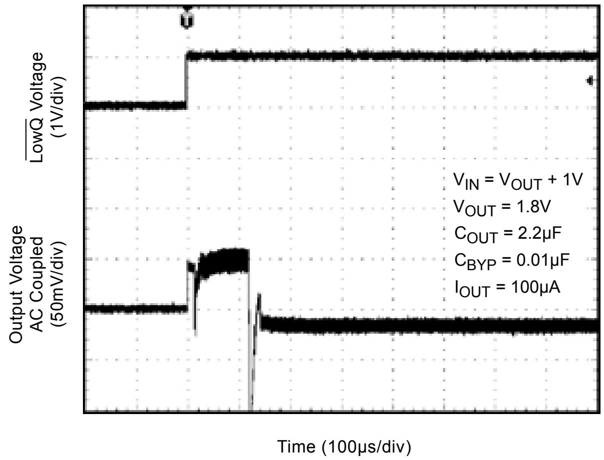


LDO2 Line Transient LowQ Mode

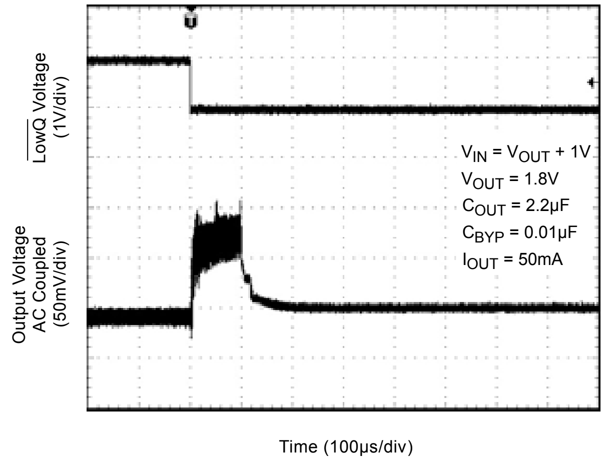


Functional Characteristics

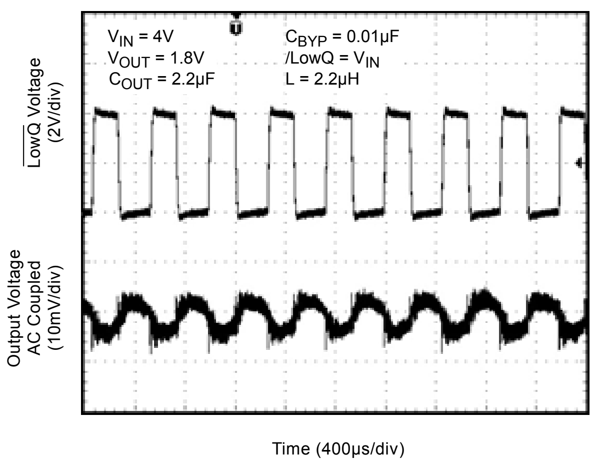
DC/DC LowQ Mode to PWM Mode Transition



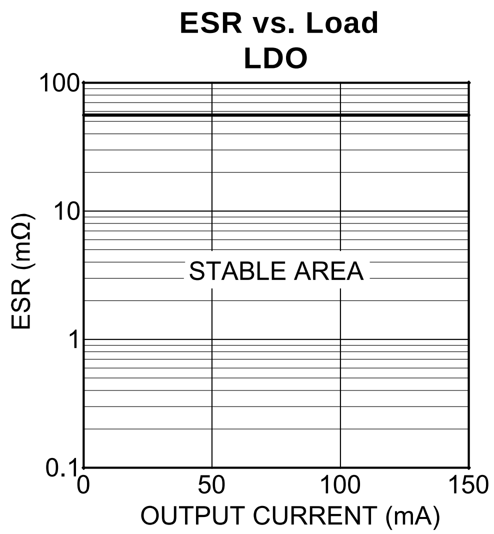
DC/DC PWM Mode to LowQ Mode Transition

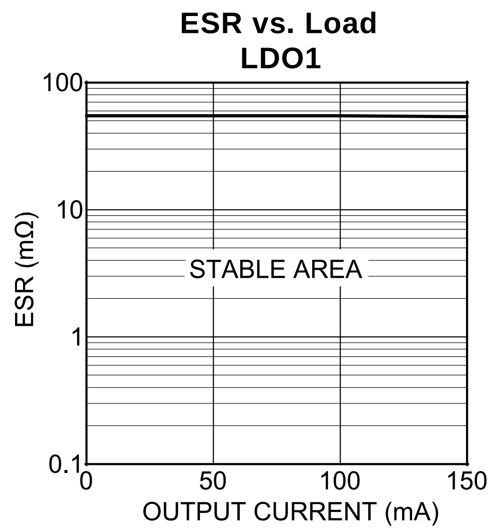


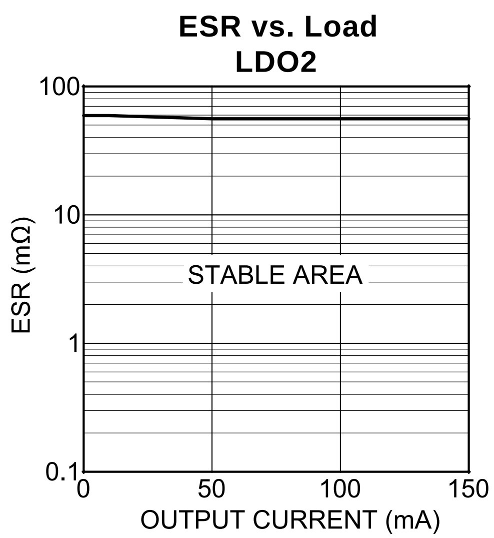
DC/DC PWM Waveform



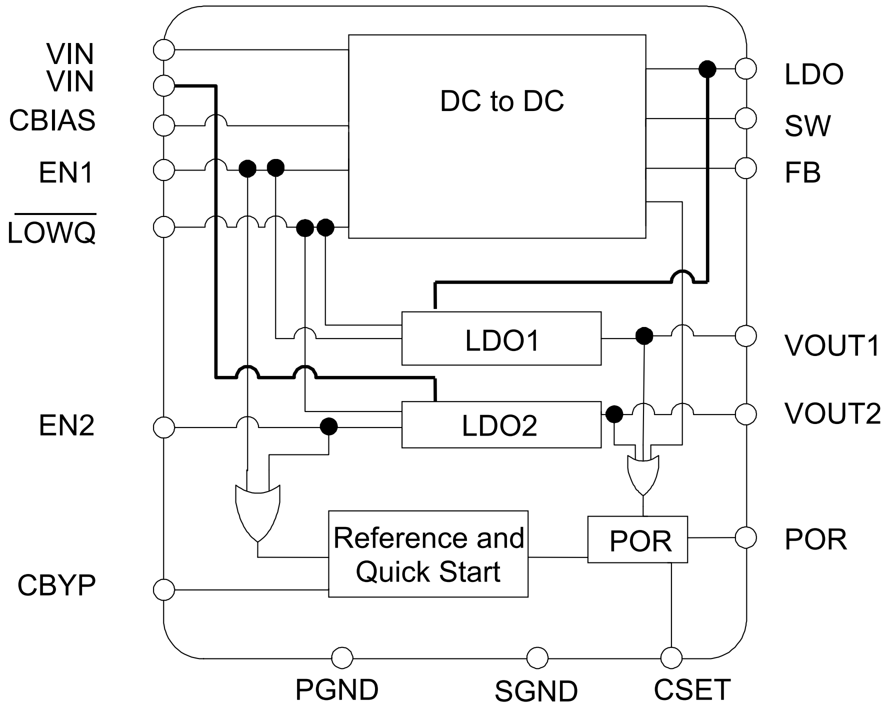
Functional Characteristics







Functional Diagram



MIC2800 Fixed Block Diagram

Application Notes

The MIC2800 is a digital power management IC with a single integrated buck regulator and two independent low dropout regulators. LDO1 is a 300mA low dropout regulator that is using power supplied by the on board buck regulator. LDO2 is a 300mA low dropout regulator using the supply from the input pin. The buck regulator is a 600mA PWM power supply that utilizes a /LOWQ light load mode to maximize battery efficiency in light load conditions. This is achieved with a /LOWQ control pin that when pulled low, shuts down all the biasing and drive current for the PWM regulator, drawing only 20µA of operating current. This allows the output to be regulated through the LDO output, capable of providing 60mA of output current. This method has the advantage of producing a clean, low current, ultra low noise output in /LOWQ mode. During /LOWQ mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM) or bursting techniques create large amplitude, low frequency ripple voltages that can be detrimental to system operation.

When more than 60mA is required, the /LOWQ pin can be forced high, causing the MIC2800 to enter PWM mode. In this case, the LDO output makes a "hand-off" to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 600mA of current to be efficiently supplied through the PWM output to the load.

VIN

Two input voltage pins provide power to the switch mode regular and LDO2 separately. The LDO1 input voltage is provided by the DC/DC LDO pin. VIN provides power to the LDO section and the bias through an internal 6Ω resistor. Both VIN pins must be tied together.

For the switch mode regulator VIN provides power to the MOSFET along with current limiting sensing. Due to the high switching speeds, a 4.7µF capacitor is recommended close to VIN and the power ground (PGND) pin for bypassing. Please refer to layout recommendations.

LDO

The LDO pin is the output of the linear regulator and should be connected to the output. In /LOWQ mode (/LOWQ <0.2V), the LDO provides the output voltage. In PWM mode (/LOWQ >1V) the LDO pin provides power to LDO1.

LDO1

Regulated output voltage of LDO1. Power is provided by the DCDC switching regulator. Recommended output capacitance is 2.2µF.

LDO2

Regulated output voltage of LDO2. Power is provided by VIN. Recommended output capacitance is 2.2µF.

EN

Both enable inputs are active high, requiring 1.0V for guaranteed operation. EN1 provides logic control of both the DCDC regulator and LDO1. EN2 provides logic control for LDO2 only. The enable inputs are CMOS logic and cannot be left floating.

The enable pins provide logic level control of the specified outputs. When both enable pins are in the off state, supply current of the device is greatly reduced (typically <1µA). When the DCDC regulator is in the off state, the output drive is placed in a "tri-stated" condition, where both the high side P-channel MOSFET and the low-side N-channel are in an “off” or non-conducting state. Do not drive either of the enable pins above the supply voltage.

Power-On Reset (POR)

The power-on reset output is an open-drain N-Channel device, requiring a pull-up resistor to either the input voltage or output voltage for proper voltage levels. The POR output has a delay time that is programmable with a capacitor from the CSET pin to ground. The delay time can be programmed to be as long as 1 second.

/LOWQ

The /LOWQ pin provides a logic level control between the internal PWM mode and the low noise linear regulator mode. With /LOWQ pulled low (<0.2V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical IQ of 20µA. In linear (LDO) mode the output can deliver 60mA of current to the output. By placing /LOWQ high (>1V), the device transitions into a constant frequency PWM buck regulator mode. This allows the device the ability to efficiently deliver up to 600mA of output current at the same output voltage.

/LOWQ mode also limits the output load of both LDO1 and LDO2 to 10mA.

BIAS

The BIAS pin supplies the power to the internal control and reference circuitry. The bias is powered from AVIN through an internal 6Ω resistor. A small 0.1µF capacitor is recommended for bypassing.

FB

Connect the feedback pin to VOUT.

SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible. Refer to the layout considerations for more details.

SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be as small as possible. Refer to the layout considerations for more details.

CSET

The SET pin is a current source output that charges a capacitor that sets the delay time for the power-on reset output from low to high. The delay for POR high to low (detecting an undervoltage on any of the outputs) is always minimal. The current source of 1.25µA charges a capacitor up from 0V. When the capacitor reaches 1.25V, the output of the POR is allowed to go high. The delay time in micro seconds is equal to the Cset in picofarads.

$$\text{POR Delay } (\mu s) = \text{CSET } (pF)$$

CBYP

The internal reference voltage can be bypassed with a capacitor to ground to reduce output noise and increase power supply rejection (PSRR). A quick-start feature allows for quick turn-on of the output voltage. The recommended nominal bypass capacitor is 0.1µF, but it can be increased, which will also result in an increase to the start-up time.

Output Capacitor

LDO1 and LDO2 outputs require a 2.2µF ceramic output capacitor for stability. The DC/DC switch mode regulator requires a 2.2µF ceramic output capacitor to be stable. All output capacitor values can be increased to improve transient response, but performance has been optimized for a 2.2µF ceramic on the LDOs and the DC/DC. X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% to 60% respectively over their operating temperature ranges.

Input Capacitor

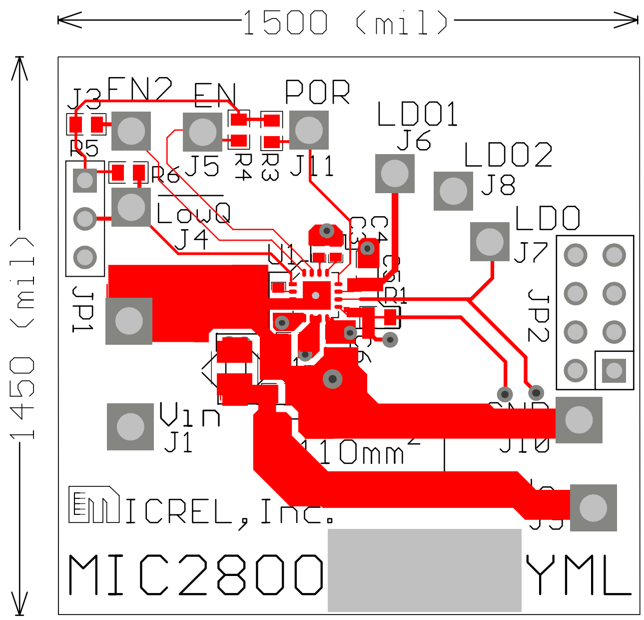
A minimum 1µF ceramic is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended. A minimum 1µF is recommended close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to layout recommendations for proper layout of the input capacitor.

Inductor Selection

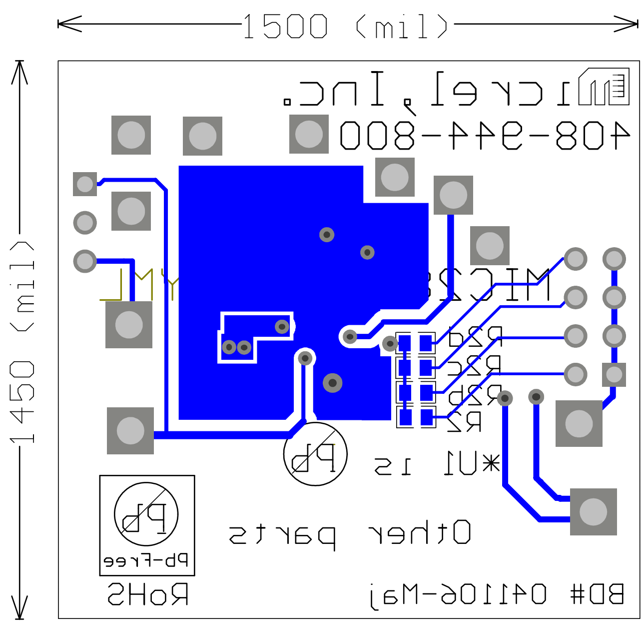
The MIC2800 is designed for use with a 2.2µH inductor. Proper selection should ensure the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

$$I_{PK} = I_{OUT} + \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \times f \times L}$$

PCB Layout

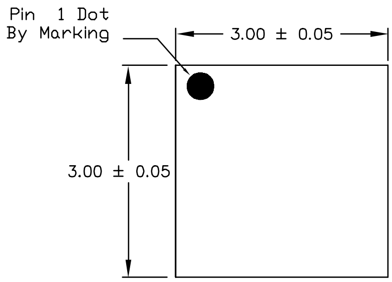


Top Layer

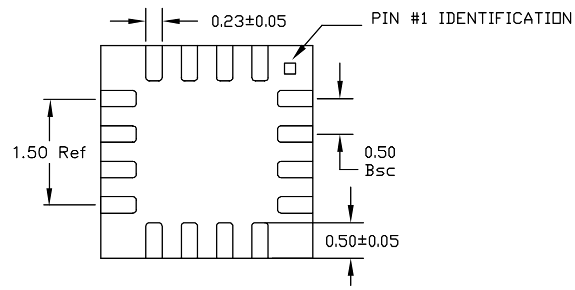


Bottom Layer

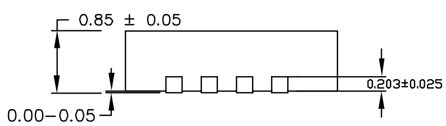
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
   N IS THE TOTAL NUMBER OF TERMINALS.
2. MAX PACKAGE WARPAGE IS 0.05mm, MAX ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
3. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin 3mm x 3mm MLF® (ML)

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