ADP1851-EVALZ User Guide
UG-443

One Technology Way P.O. Box 9106 Norwood, MA 02062-9106, U.S.A. Tel: 781.329.4700 Fax: 781.461.3113 www.analog.com

Evaluation Board for the ADP1851 Step-Down DC-to-DC Controller

FEATURES

Input voltage range: 9 V to 15 V
Output voltage: 1.8 V
Output current: up to 25 A
Switching frequency: 600 kHz
Operates in PWM or PSM
Designed for evaluation of the ADP1851 functionality
Flexible and easy to re-configure and modify

EVALUATION BOARD DESCRIPTION

This document describes the design, operation, and test results of the ADP1851-EVALZ. The input voltage range for this evaluation board is 9 V to 15 V, and the regulated output voltage (V_{OUT}) is set to 1.8 V with the maximum output current up to 25 A. The switching frequency (f_{SW}) of 600 kHz is set to achieve high efficiency. The switching frequency can be also synchronized to an external clock signal applied to the SYNC input.

ADP1851 DEVICE DESCRIPTION

The ADP1851 is a step-down switching controller with integrated drivers for N-channel synchronous power MOSFETs.

The ADP1851 can be set to operate in pulse skip mode (PSM) for high efficiency under light load, or in PWM continuous conduction mode. In addition, the boost diode is integrated into the ADP1851, thus lowering the overall system cost and component count.

The ADP1851 includes externally adjustable soft start, output overvoltage protection, externally programmable current limit, power good output, and a programmable oscillator frequency that ranges from 200 kHz to 1.5 MHz. The switching frequency of the ADP1851 can be synchronized to an external clock signal applied to the SYNC input. The ADP1851 has the reference voltage accuracy of ±1% from −40°C to +125°C junction temperature. This controller can be powered from a 2.75 V to 20 V supply and is available in a 16-lead 4 mm × 4 mm LFCSP package.

ADP1851 EVALUATION BOARD

Figure 1.

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REVISION HISTORY

8/12—Revision 0: Initial Version

COMPONENT DESIGN

ADIsimPower DESIGN TOOL

The ADP1851 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized to a specific design goal. The tools allow the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/ADIsimPower and users can request an unpopulated board through the tool.

For information about selecting power components and calculating component values, see also the ADP1851 data sheet.

INDUCTOR SELECTION

The selected inductor is a Coilcraft SER1408-301ME with 0.3 µH inductance, and 53 A saturation current. This shielded inductor with a flat wire windings core provides exceptionally low DCR of 0.5 mΩ (typical).

INPUT CAPACITORS

Because of the low ESR and high input current rating of a multilayer ceramic capacitor (MLCC), a 10 µF MLCC is selected as the input capacitor close to the high-side power MOSFET. In addition, a 150 µF bulk OS-CON™ capacitor (aluminum solid capacitor with conductive polymer) from Sanyo is chosen for filtering out any unwanted low frequency noise from the input power supply.

OUTPUT CAPACITORS

A combination of the 330 µF POSCAP™ polymer capacitors and the 47 µF MLCC is selected for the output rail. Polymer capacitors have low ESR and high current ripple rating. Connecting polymer capacitors and MLCCs in parallel is very effective in reducing voltage ripple.

MOSFET SELECTION

For low output or low duty cycle, select a high-side MOSFET with fast rise and fall times and with low input capacitance to minimize charging and switching power loss. As for the synchronous rectifier (low-side MOSFET), select a MOSFET with low R_{DSON} because it conducts current most of the time during the switching cycle and contributes a larger portion in the conductive losses than the high-side MOSFET. For the high-side MOSFET, two BSC052N03LS from Infineon in the PG-TDSON-8 package are selected. These parts have low input capacitance (770 pF typical) and fast transition times (typical turn-on delay is 2.4 ns). For the low-side MOSFET, two BSC090NS from Infineon, with the R_{DSON} of 3.5 mΩ (maximum at V_{GS} of 4.5 V) are selected.

TEST RESULTS

T_A = 25°C.

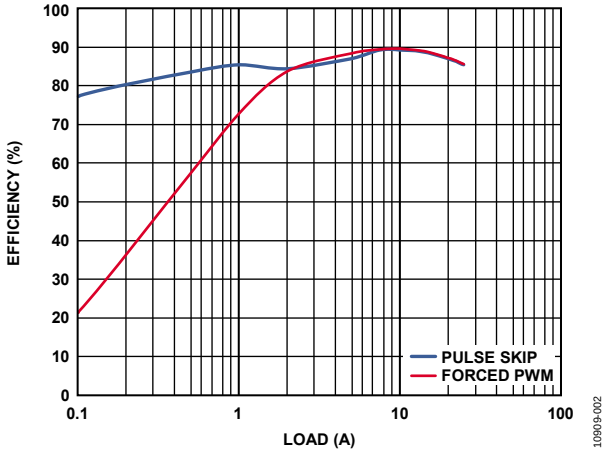

Figure 2. Efficiency, V_{IN} = 12 V, V_{OUT} = 1.8 V, f_{OSC} = 600 kHz

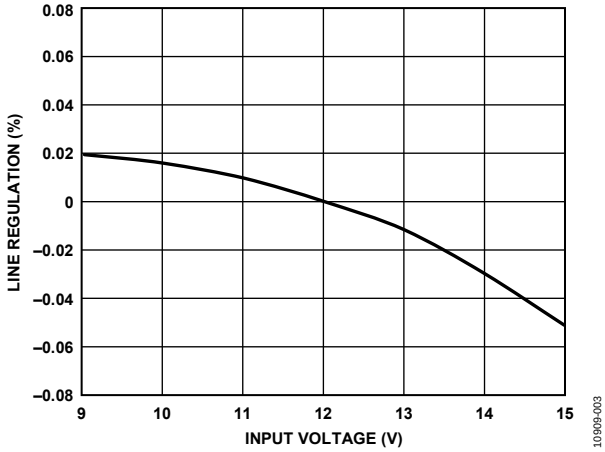

Figure 3. Line Regulation, V_{OUT} = 1.8 V, f_{SW} = 600 kHz, 25 A Load

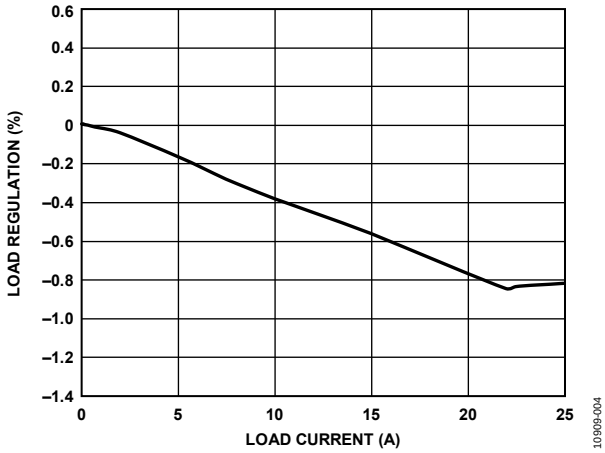

Figure 4. Load Regulation, V_{IN} = 12 V, V_{OUT} = 1.8 V, f_{SW} = 600 kHz

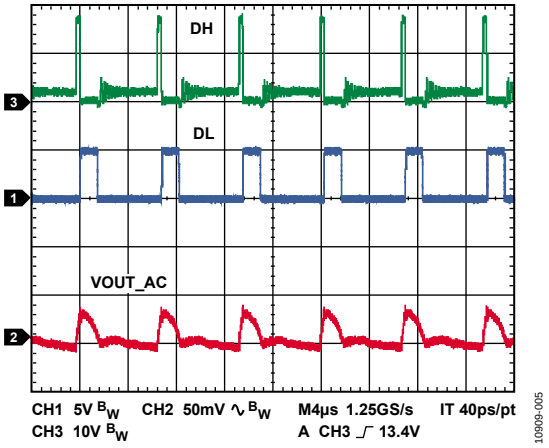

Figure 5. Switching Waveforms, Light Load of 1.5 A, f_{OSC} = 600 kHz, Pulse Skip Enabled, SYNC Low

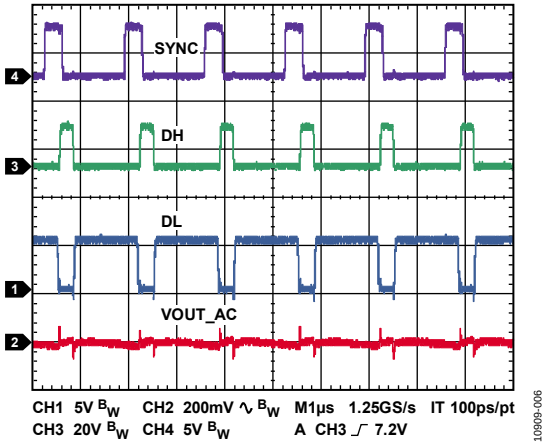

Figure 6. Switching Waveforms, 25 A Load, f_{SYNC} = 600 kHz

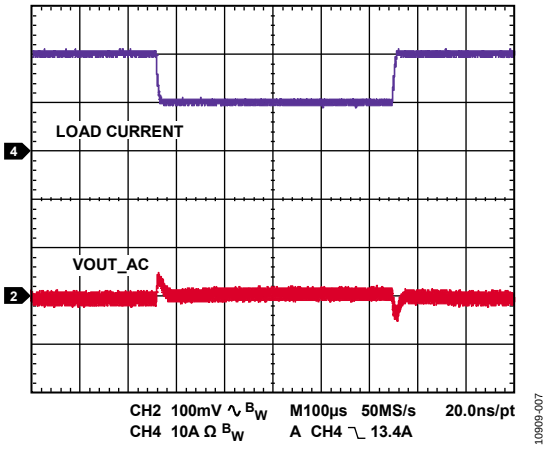

Figure 7. V_{OUT} Transient Response, 20 A to 10 A Load Step

EVALUATION BOARD OPERATING INSTRUCTION

1. Connect Jumper JP2 (EN) with a shunt to the low position (disabled).
2. Connect Jumper JP1 (FRQ) with a shunt to the high position for 600 kHz operation.
3. Connect Jumper JP5 (SYNC) with a shunt to the high position for PWM operation or to the low position for pulse skip operation at light load.
4. Remove Jumper JP4 (TRK) for the soft-start operation.
5. Connect a power supply to the board input terminals VIN+ and GND and apply 12 V.
6. Connect Jumper JP2 (EN) to the high position to enable the ADP1851.

Table 1. Jumper Description

Jumper	Description	Default Factory Setting	Function
JP1	FRQ	Low	Connect shunt low for 300 kHz or high for 600 kHz switching frequency operation. The ADP1851-EVALZ is configured for operation at 600 kHz. Connect JP1 high.
JP2	EN	Low	Connect shunt high to enable the ADP1851 or low to disable it.
JP4	TRK	Open	Keep open to study the soft-start function. Short with shunt to study the tracking capability when the master voltage is applied to TP18 (TRK_IN) and divided with the R8/R9 resistors.
JP5	SYNC	Low	Connect shunt high for PWM or low for pulse skip operation. For synchronization, remove the shunt from JP5 and apply an external clock to the TP12 SYNC.

Table 2. Performance Summary (T_A = 25°C)

Parameter	Condition
V_{IN}	9 V to 15 V
f_{SW}	Switching frequency, 600 kHz
V_{OUT}	1.8 V
I_{OUT}	0 A to 25 A
V_{OUT} Ripple, DC Load	35 mV at 25 A load
V_{OUT} Deviation upon Step Load Release	2.5% with 10 A step load

OTHER INFORMATION ABOUT THE EVALUATION BOARD PCB LAYOUT

As seen in Figure 1, the layout of this evaluation board is not optimized for the smallest PCB area. It is laid out in such a way that any of the components can be desoldered and replaced easily with different components by using a hand soldering iron so that the user can modify the existing design without acquiring a new PCB layout. The physical size of the compensation components is 0603, which is selected for its ease of hand soldering when reworking the board is needed. The size of these components can be smaller in an actual design. The user can also remove or change any of the power components, including the output filter capacitors, high-side and low-side MOSFETs, input capacitors, and inductor, to achieve a particular design objective. If a tracking function is needed, the user can remove Capacitor C6, place a resistor divider (R8/R9) to configure the desired tracking function, and short the JP4 (TRK) with shunt. To study the precision enable function, remove the shunt from JP2 and apply an external voltage to TP2 EN. To program a higher UVLO threshold, place the required resistor divider (R3/R5).

See Figure 8, the evaluation board schematic, for more information.

EVALUATION BOARD SCHEMATICS AND ARTWORK

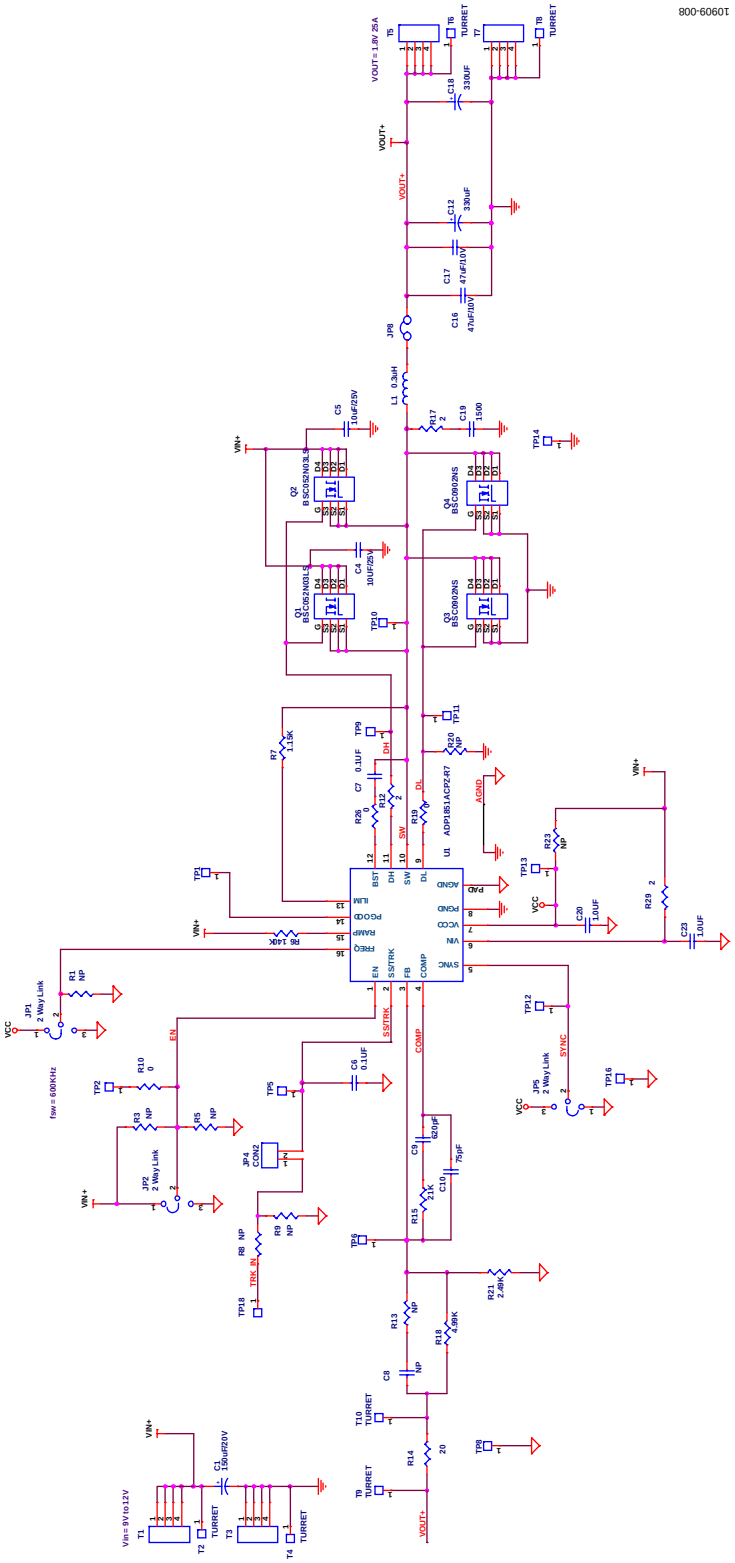

Figure 8. Evaluation Board Schematic

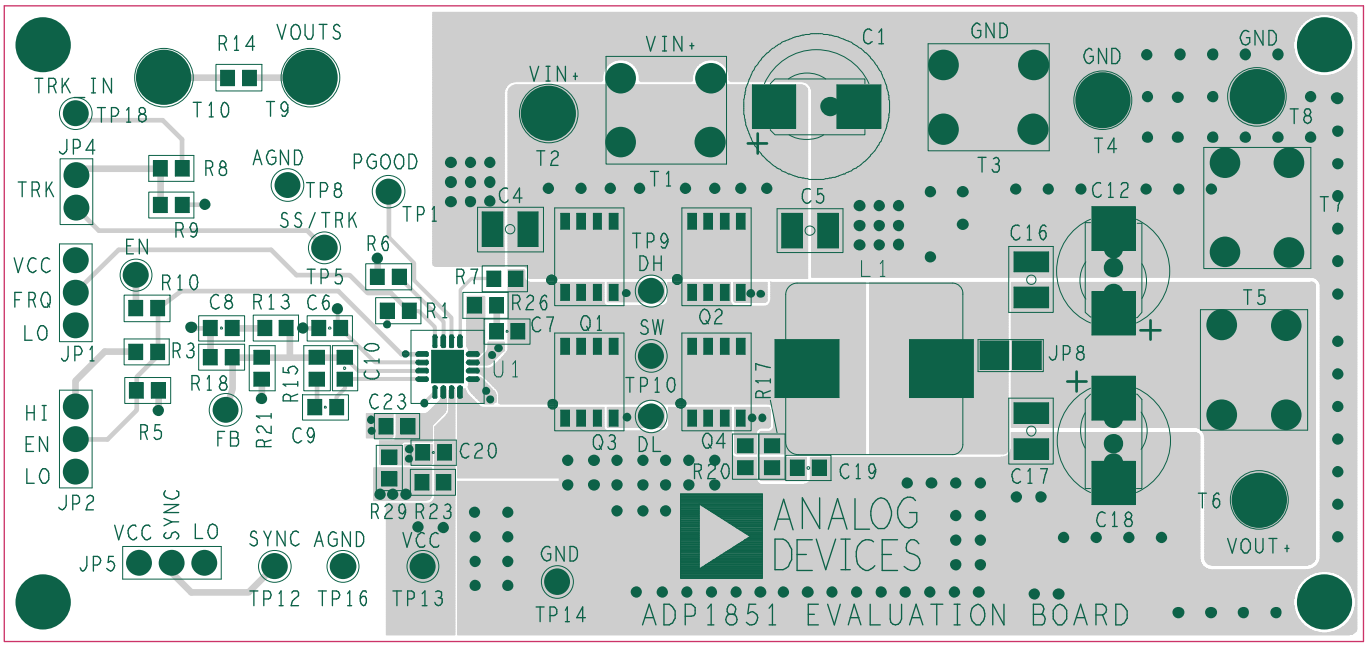

Figure 9. Top Layer with Silkscreen

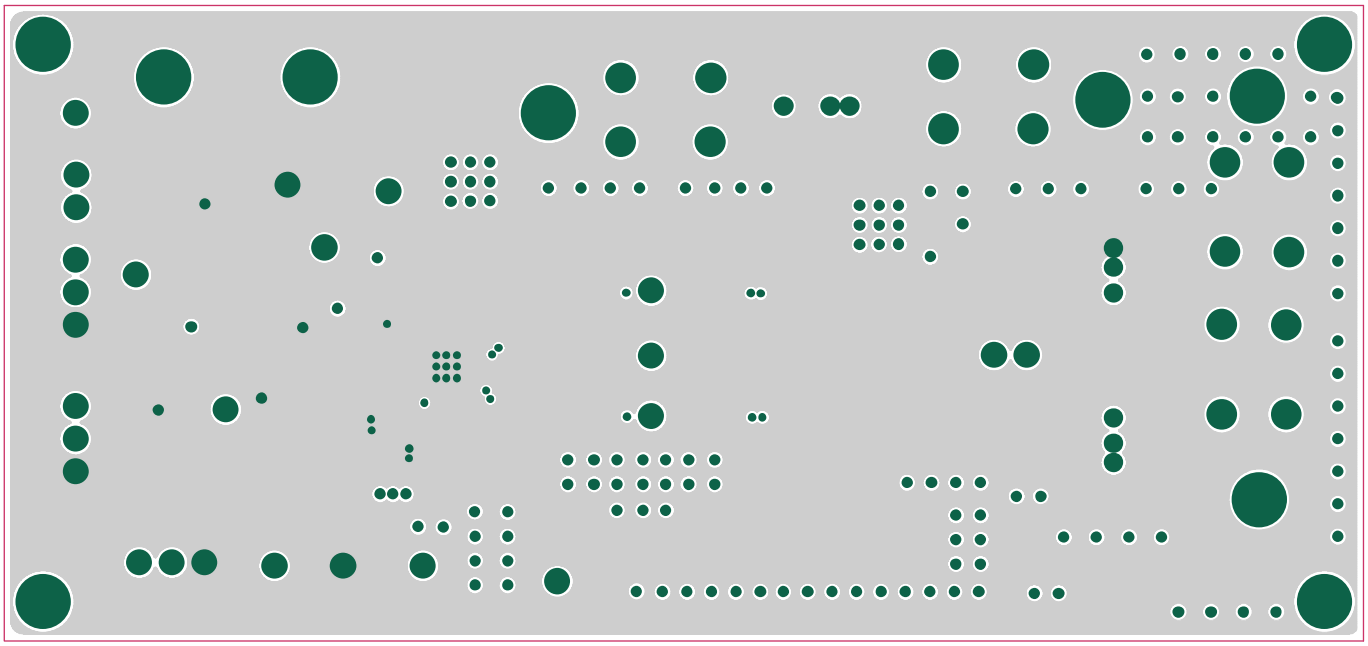

Figure 10. Second Layer (AGND Plane)

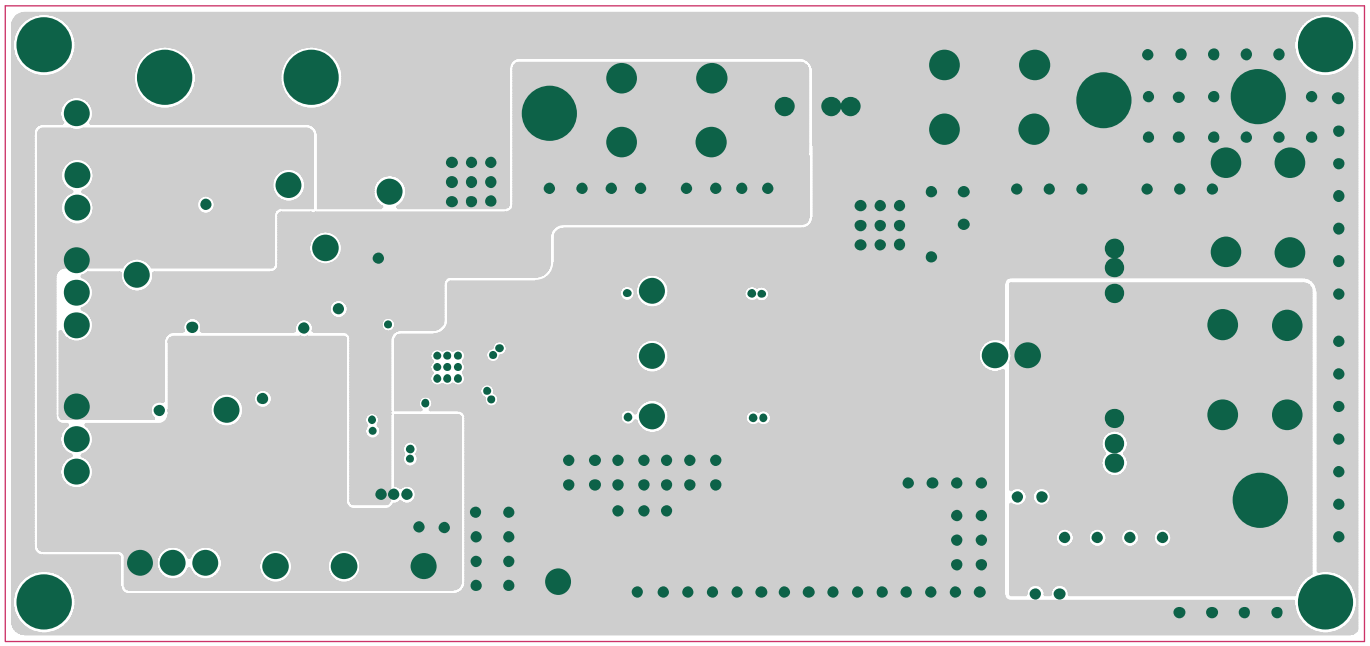

Figure 11. Third Layer (V_{IN}, V_{CCO}, V_{OUT}, and PGND)

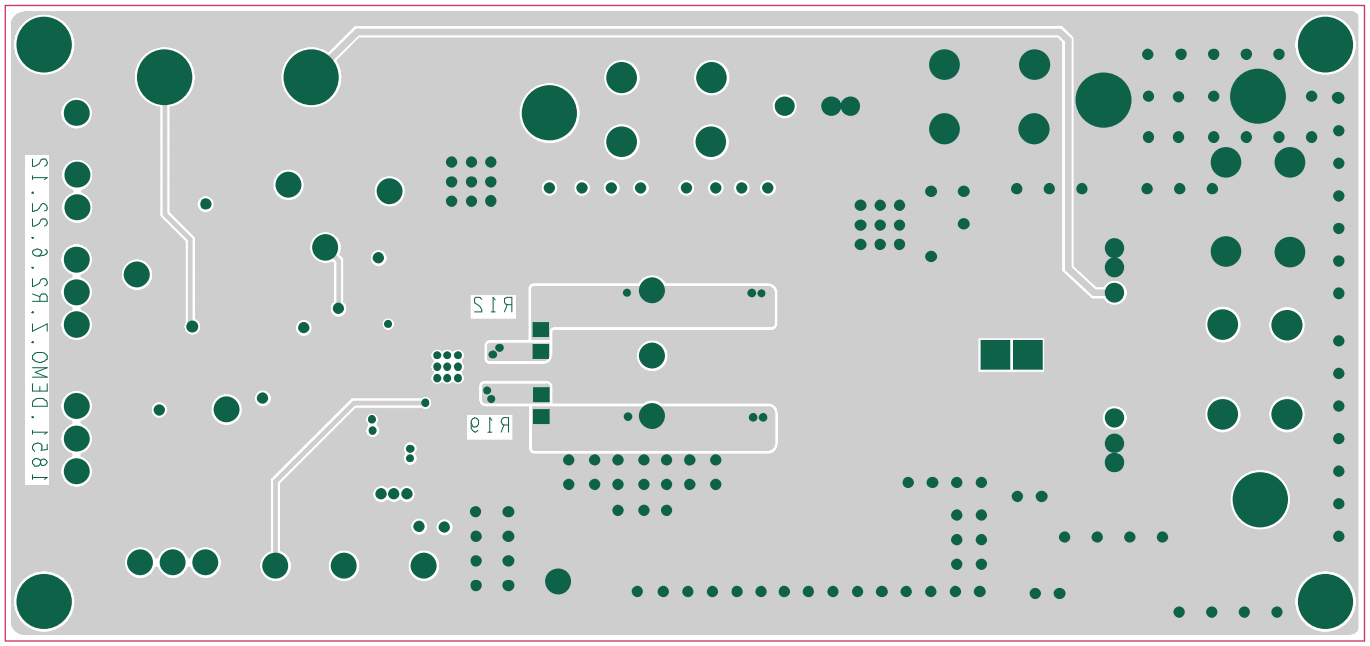

Figure 12. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Manufacturer	Part No.
1	C1	OS-CON 150 µF 20 V	Sanyo	20SEP150M
2	C4, C5	Capacitor ceramic 10 µF 25 V 10% X7R 1210	Murata	GRM32DR71E106KA12
2	C6, C7	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603	Murata	GRM188R71E104KA01D
1	C8	Open		
1	C9	Capacitor ceramic 620 pF C0G/NP0 0603	Murata	GRM1885C1H621JA01D
1	C10	Capacitor ceramic 75 pF C0G/NP0 0603	Murata	GRM1885C1H750JA01D
2	C12, C18	POSCAP 330 µF 2.5 V 7 mΩ	Sanyo	2R5TPE330M7
2	C16, C17	Capacitor ceramic 47 µF 10 V X5R 1210	Murata	GRM32ER61A476KE20L
1	C19	Capacitor ceramic 1500 pF X7R 0603	Murata	GRM188R71H152KA01D
2	C20, C23	Capacitor ceramic 1 µF 25 V X7R 0603	Murata	GRM188R71E105KA12D
3	JP1, JP2, JP5	Jumper, Header 3, 0.100'	Samtec	TSW-150-07-G-S
1	JP4	Jumper, Header 2, 0.100'	Samtec	TSW-150-07-G-S
1	JP8	Solder bridge		
1	L1	Inductor 0.3 µH 0.5 mΩ, I_{SAT} = 53 A, I_{RMS} = 42 A	Coilcraft	SER1408-301ME
2	Q1, Q2	N MOSFET, 30 V, 5.2 mΩ	Infineon	BSC052N03LS
2	Q3, Q4	N MOSFET, 30 V, 2.6 mΩ	Infineon	BSC0902NS
8	R1, R3, R5, R8, R9, R13,R20, R23	Open		
1	R6	Resistor 140 kΩ 1%	Vishay	CRCW0603140KFKEA
1	R7	Resistor 1.15 kΩ 1%	Vishay	CRCW06031K15FKEA
3	R10, R19, R26	Resistor 0 Ω	Vishay	CRCW06030000Z0EA
3	R12, R17, R29	Resistor 2.0 Ω 1%	Vishay	CRCW0602R00FKEA
1	R14	Resistor 20 Ω	Vishay	CRCW060320R0FKEA
1	R15	Resistor 21.0 kΩ 1%	Vishay	CRCW060321K0FKEA
1	R18	Resistor 4.99 kΩ 1%	Vishay	CRCW06034K99FKEA
1	R21	Resistor 2.49 kΩ 1%	Vishay	CRCW06032K49FKEA
13	TP1, TP2, TP5, TP6, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP16, TP18	Test points, header 0.100"	Samtec	TSW-150-07-G-S
4	T1, T3, T5, T7	Terminal screw vertical PC MNT	Keystone Electronics Corp.	8191K-ND
6	T2, T4, T6, T8, T9, T10	TURRET170	Keystone Electronics Corp.	1502-1
1	U1	Device under test, 16-lead LFCSP	Analog Devices	ADP1851ACPZ-R7
4		Shunt	Samtec	SNT-100-BK-G
4		Standoff HEX .500/4 NYL	Keystone Electronics Corp.	1902C
4		Screw NYL slot	Richco	NSS-4-6-01

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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