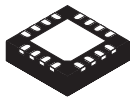
Document Number: MC34933
Rev. 2.0, 7/2010

RoHS

1.4 A Dual H-Bridge Driver Compatible with 3.0 V Logic

34933

H-BRIDGE DRIVER



EP SUFFIX (Pb-FREE)
98ASA00110D
16-PIN UQFN

The 34933 is a two channel H-Bridge driver aimed at the digital camera market. There are a variety of applications containing bipolar step motors and/or brush DC motors, such as Auto Focus control for the digital camera lens. The 34933 uses Freescale's proprietary SMOS8 Bi CMOS process to deliver a low power device, with a maximum quiescent current of 100 μA for the motor drive supply and 400μA for the Control Logic supply.

The 34933 V_M supply operates from 2.0 V to 7.0 V using an internal charge pump, with independent control of each H-Bridge driver via the MCU (IN1A, IN1B, IN2A, IN2B). The 34933 has a low total RDS_{ON} of 1.0 Ω (Max. at 25 °C). Shoot-through current protection is a built-in feature for the 34933 device.

The 34933 has four operation modes: Forward, Reverse, Brake, and Tri-State (High Impedance). The 34933 employs a VCC detection circuit to sense when the logic supply switches to an off-state with a maximum current of 1uA to extend battery life. The H-Bridge drivers can be independently pulse width modulated up to 200 kHz for speed/ torque and/or current control. Note that Tri State Mode of H-Bridge drivers can occur when either VCC Detect is low or the Thermal Detect is active.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34933EP/R2	-20 °C to 85 °C	16-UQFN

Features

- Built-In 2-Channel H-Bridge Driver
- H-Bridge Operation Voltage 2.0 V~7.0 V
- Max. Load Output Current 1.0 A @ T_A = 25 °C
- Low Total RDS_{ON} 0.8 Ω (Typ), 1.0 Ω (Max.) @ T_A = 25 °C Peak
- Dual Channel Parallel Driver, RDS_{ON} 0.4 Ω (Typ.). Max. DC Current 1.4 A
- PWM Control Input Frequency up to 200 kHz
- Built-In Shoot-Through Current Prevention Circuit
- Built-In Charge Pump Circuit (External Cap type)
- VCC Low Voltage Detection for logic power supply voltage
- Thermal Detection for H-Bridge driver

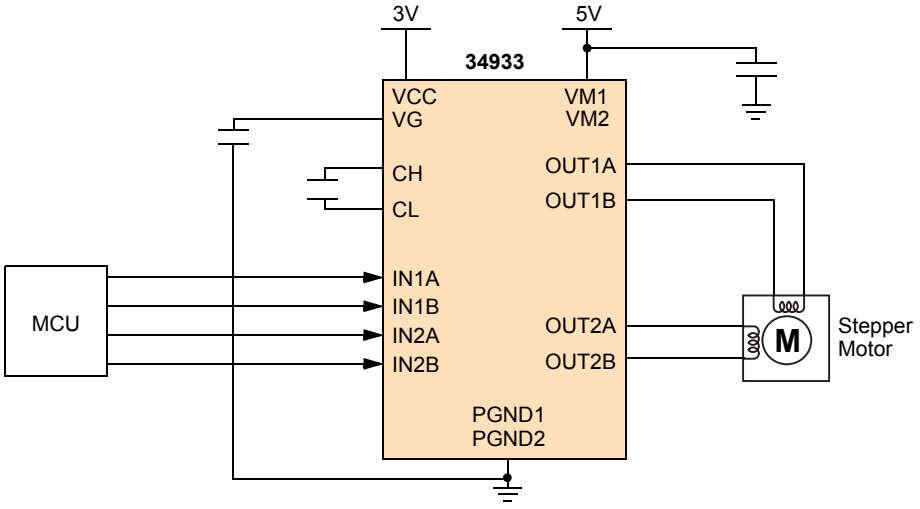


Figure 1. 34933 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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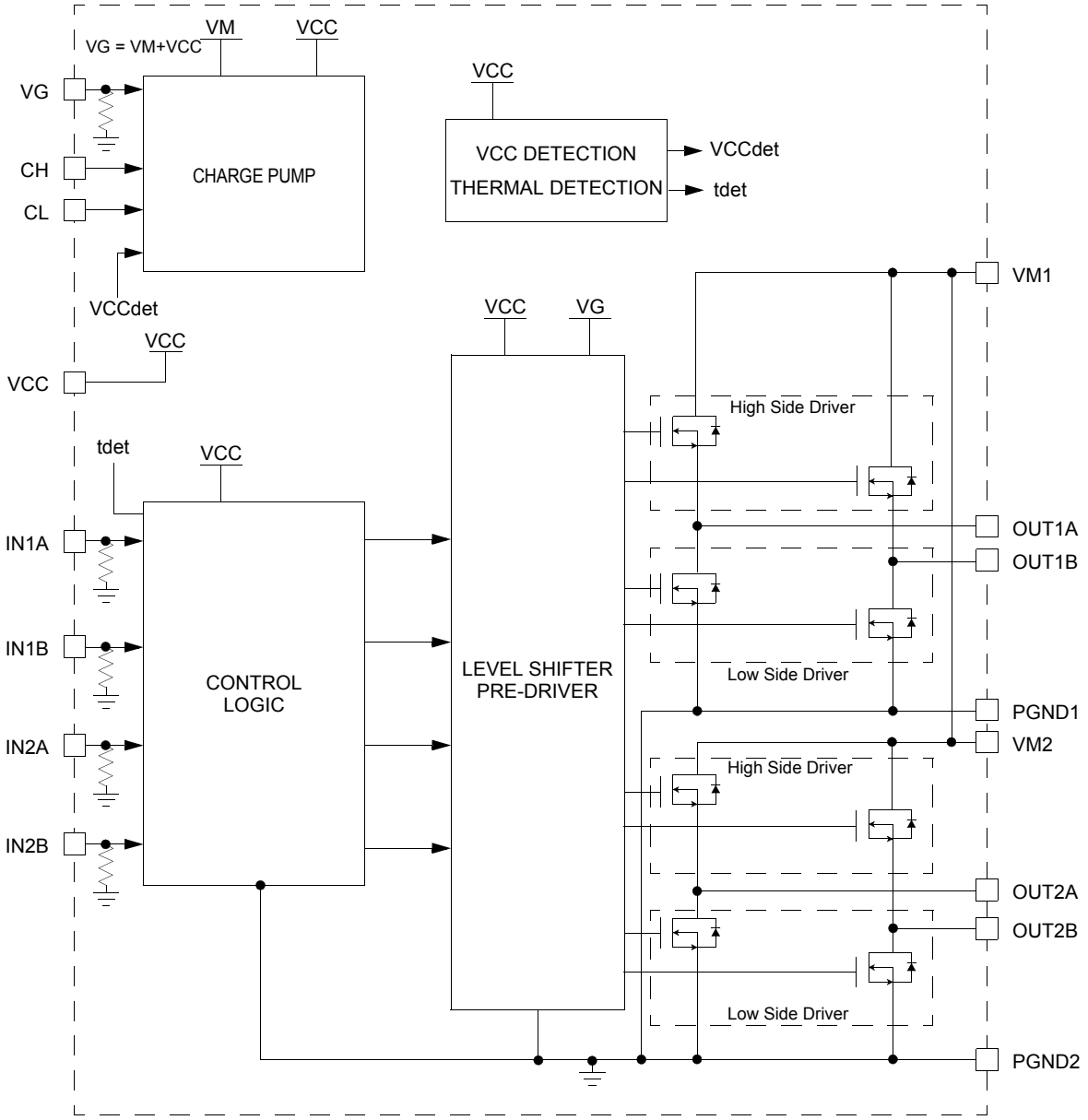
INTERNAL BLOCK DIAGRAM



* VM1 and VM2 are connected internally. Both VM1 and VM2 must be tied together on the PCB.
PGND1 and PGND2 are connected internally. Both PGND1 and PGND2 must be tied together on the PCB.

Figure 2. 34933 Simplified Internal Block Diagram

PIN CONNECTIONS

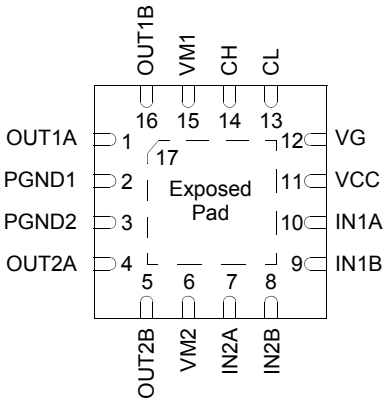


Figure 3. 34933 Pin Connections

Table 1. 34933 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	OUT1A	Output	H-Bridge output 1A	Output A of H-Bridge channel 1.
2	PGND1	Power supply	Power ground 1	Power Supply Grounds for the 34933 device. Please refer to the Application Diagram for recommended layout.
3	PGND2	Power supply	Power ground 2	Power Supply Grounds for the 34933 device. Please refer to the Application Diagram for recommended layout.
4	OUT2A	Output	H-Bridge output 2A	Output A of H-Bridge channel 2
5	OUT2B	Output	H-Bridge output 2B	Output B of H-Bridge channel 2
6	VM2	Power supply	Motor drive power supply 2	Power Supply pins for the 34933 Motor Drive circuitry. Please refer to the Application diagram for recommended layout.
7	IN2A	Input	Logic input control 2A	Logic input control of OUT2A
8	IN2B	Input	Logic input control 2B	Logic input control of OUT2B
9	IN1B	Input	Logic input control 1B	Logic input control of OUT1B
10	IN1A	Input	Logic input control 1A	Logic input control of OUT1A
11	VCC	Power supply	Control logic power supply	Power Supply for the Control Logic circuitry.
12	VG	Output	Charge pump output capacitor	Charge Pump Output pin connected to an external capacitor. Note the VG voltage is the sum of the VCC and VM power supplies.
13	CL	Input/Output	Charge pump capacitor 1	Low side Charge Pump capacitor connection
14	CH	Input/Output	Charge pump capacitor 2	High side Charge Pump capacitor connection
15	VM1	Power supply	Motor drive power supply 1	Power Supply pins for the 34933 Motor Drive circuitry. Please refer to the Application diagram for recommended layout.
16	OUT1B	Output	H-Bridge output 1B	Output B of H-Bridge channel 1
17[(1)]	Exposed Pad	Power supply	EP	The Exposed Pad is connected to Ground plane via the Exposed Pad solder pad. Note the primary purpose of the Exposed pad for 34933 is thermal heat dissipation. Therefore, adequate thermal vias should be included in the PCB design.

Notes
1. Exposed pad is used as a heat sink. Connect it to the power ground through four thermal vias where the area is wide.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Control Logic Power Supply Voltage	VCC	-0.5 to +6.0	V
Motor Drive Power Supply	VM	-0.5 to +7.5	V
VCC Level Terminal Voltage - IN1A, IN1B, IN2A, IN2B	Vterminal1	-0.5 to +5.5	V
VM Level Terminal Voltage - OUT1A, OUT1B, OUT2A, OUT2B, CL	Vterminal2	-0.5 to +7.5	V
VM+VCC Level Terminal Voltage - CH, VG	Vterminal3	-0.5 to +13.5	V
Motor Drive Maximum Load Current, T_A = 85 °C	Iload_dc_MD	0.7	A
Motor Drive Maximum Load Current, T_A = 25 °C	Iload_dc_MD	1.0	A
Motor Drive Maximum Peak Load Current[3]	Iload_peak_MD	1.4	A
Power Dissipation[4]	PD	1.0	W
ESD Voltage[2]	V_{ESD}		V
Human Body Model (HBM)		±4000	
Machine Model (MM)		±350	
Charge Device Model (CDM)		±1000	
THERMAL RATINGS			
Operating Temperature Range	T_A	-20 to +85	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	Tstg	-65 to +150	°C
THERMAL RESISTANCE			
Thermal Resistance, Junction to Case[5]	$R_{\theta JC}$	23	°C/W
Peak Package Reflow Temperature During Reflow[6], [7]	T_{PPRT}	Note 7	°C

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 W), the Machine Model (MM) (CZAP = 200 pF, RZAP = 0 W), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).
3. Peak time is for 10ms pulse width at 200ms intervals. T_A = 25°C.
4. RθJA = 50 °C/W, in case of 2s2p printed-circuit board that defined on SEMI JEDEC JESD51- 3 and JESD51-6.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS

Table 3. Static and Dynamic Electrical Characteristics

Characteristics noted under conditions, VM = 5.0 V, VCC = 3.0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Motor Drive Power Supply Voltage	V_M	2.0	5.0	7.0	V
Control Logic Power Supply Voltage	V_{cc}	2.7	3.0	5.5	V
Driver Quiescent Supply Current (IN1A, IN1B,IN2A, IN2B = L) No Signal Input	I_{QM}	- 	72 	100 	uA
Logic Quiescent Supply Current (IN1A, IN1B, IN2A, IN2B = L) No Signal Input	I_{QVCC}	- 	114 	400 	uA
Control Logic Power Supply Operating Current (IN1A, IN2A = L, IN1B, IN2B = 200kHz)	I_{VCC}	-	350	800	uA
Charge Pump Target Voltage VM = 2.0 V, VCC = 2.7 V, I_{LOAD} = 0A VM = 5.0 V, VCC = 3.0 V, I_{LOAD} = 0A VM = 7.0 V, VCC = 5.5 V, I_{LOAD} = 0A	V_G	 4.2 7.6 12.0	 4.45 7.8 12.3	 4.7 8.0 12.5	V
Charge Pump Wake Up Time Charge pump is enabled in VCC>Vccdet	T_{VGON}	 	 130	 400	us
Driver Quiescent Supply Current at VCCDET = L V_M = 5.0 V, V_{CC} = 0 V	$I_{QM\_VCD = L}$	- 	- 	1.0 	uA
Charge Pump Switching Frequency	F_{QP}	-	150	-	KHz
H-BRIDGE DRIVER					
H-Bridge Driver High/Low Side Driver On-Resistance 1 V_{CC} = 2.7 V, Isink = 100 mA, T_A = 25°C	Ron1	- 	0.4 	0.45 	Ω
H-Bridge Driver High/Low Side Driver On-Resistance 2[8] V_{CC} = 2.7 V, Isink = 700mA, T_A = 25°C	Ron2	- 	0.43 	0.51 	Ω
H-Bridge Driver High/Low Side Driver On-Resistance 3[8] V_{CC} = 2.7 V, Isink = 700mA, T_A = 85°C	Ron3	- 	0.51 	0.62 	Ω
H-Bridge Driver High/Low Side Driver On-Resistance 4 V_{CC} = 3.0 V, Isink = 100mA, T_A = 25°C	Ron4	- 	0.39 	0.43 	Ω
H-Bridge Driver High/Low Side Driver On-Resistance 5[8] V_{CC} = 3.0 V, Isink = 700mA, T_A = 25°C	Ron5	- 	0.41 	0.48 	Ω
H-Bridge Driver High/Low Side Driver On-Resistance 6 [8] V_{CC} = 3.0 V, Isink = 700mA, T_A = 85°C	Ron6	- 	0.49 	0.58 	Ω
H-Bridge Driver Output Body Diode Forward Voltage I_f = 100 mA	V_f	- 	0.8 	1.2 	V
Input Pulse Frequency (INA/B) Duty of input signal = 50 %	F_{IN}	- 	- 	200 	kHz

Notes

8. Guaranteed by design

Table 3. Static and Dynamic Electrical Characteristics

Characteristics noted under conditions, VM = 5.0 V, VCC = 3.0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{A=}$ 25 °C under nominal conditions, unless otherwise noted.

H-Bridge Output Propagation Delay Time for OUTA/B (H to L) Rload = (1 kΩ) between OUTA and OUTB (refer to Figure 4) (IN1A, IN2A = L, IN1B, IN2B = 200 kHz)	t_{PDHL}	-	0.1	0.5	us
H-BRIDGE DRIVER (CONTINUED)					
H-Bridge Output Propagation Delay Time for OUTA/B (L to H) Rload = (1k Ω) between OUTA and OUTB (refer to Figure 4) (IN1A, IN2A = L, IN1B, IN2B = 200 kHz)	t_{PDLH}	-	0.1	0.5	us
H-Bridge Output Pulse Width Rload = 20 Ω between OUTA and OUTB, Input Pulse Width = 1.0us, 50% to 50%, t_{PW}: 50% to 50% (refer to Figure 5)	t_{PW}	0.7	-	-	us
H-Bridge Output Propagation Delay Time (Hi-Z to H) (8) Rload = 100 kΩ to 1/2*VM, Cload = 0 pF, t_{PDZH} 50% to 75%	t_{PDZH}	-	-	0.5	us
H-Bridge Output Propagation Delay- Time (H to Hi-Z) (8) Rload = 100 kΩ to 1/2*VM, Cload = 0 pF, t_{PDHZ} 75% to 50%	t_{PDHZ}	-	-	2.0	us
CONTROL LOGIC					
High Level Input Voltage (IN1A, IN1B, IN2A, IN2B) Vcc = 2.7 V ~ 5.5 V	V_{IH}	V_{CC}x0.7	-	-	V
Low Level Input Voltage (IN1A, IN1B, IN2A, IN2B) Vcc = 2.7 V ~ 5.5 V	V_{IL}	-	-	V_{CC}x0.3	V
High Level Input Current (IN1A, IN1B, IN2A, IN2B) Vtermainal1 = 3.0 V	I_{IH}	9	-	20	uA
Low Level Input Current (IN1A, IN1B, IN2A, IN2B) Vcc = 2.7 V ~ 5.5 V	I_{IL}	-1.0	-	-	uA
Input Pulse Rise Time (IN1A, IN1B, IN2A, IN2B) Vcc = 2.7 V ~ 5.5 V	tr	-	-	1.0	us
Input Pulse Fall Time (IN1A, IN1B, IN2A, IN2B) Vcc = 2.7 V ~ 5.5 V	tf	-	-	1.0	us
DETECTOR					
VCC Detection Voltage (refer to Figure 6)	Vccdet	2.0	2.2	2.4	V
VCC Detection hysteresis Voltage (refer to Figure 6)	Vccdethys	0.05	0.1	0.3	V
Thermal Detection Temperature (9)	Tdet	150	170	190	°C
Thermal Detection Hysteresis Temperature (9)	Tdethys	10	20	30	°C

Notes
9. Guaranteed by design

TIMING DIAGRAMS

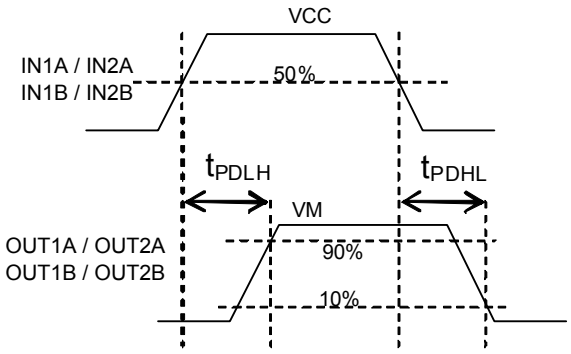


Figure 4. t_{PDLH} and t_{PDHL} Timing

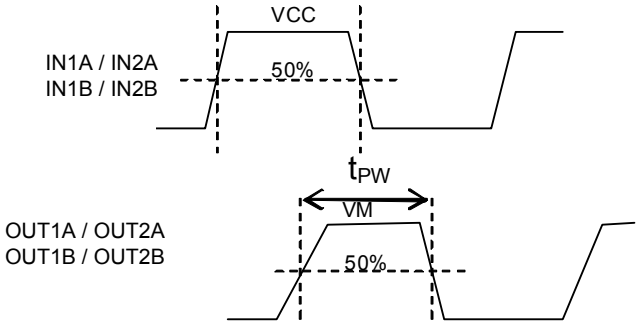


Figure 5. t_{PW} Timing

Table 4. Truth Table

		INPUT		OUTPUT	
Vccdet	Tdet	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B
L	X	X	X	Z	Z
H	L	L	L	L	L
H	L	H	L	H	L
H	L	L	H	L	H
H	L	H	H	Z	Z
H	H	X	X	Z	Z

H - High
L - Low
Z - High Impedance
X - Don't Care

Figure 6 and Figure 7 show the timing charts of input and output signals

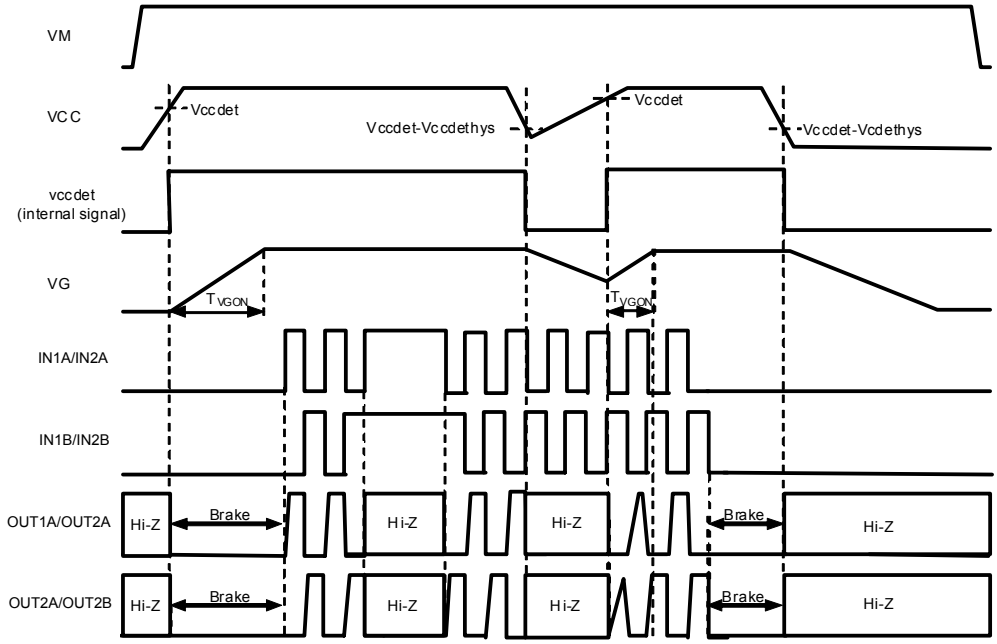


Figure 6. Timing chart of input and output signal (Vccdet case)

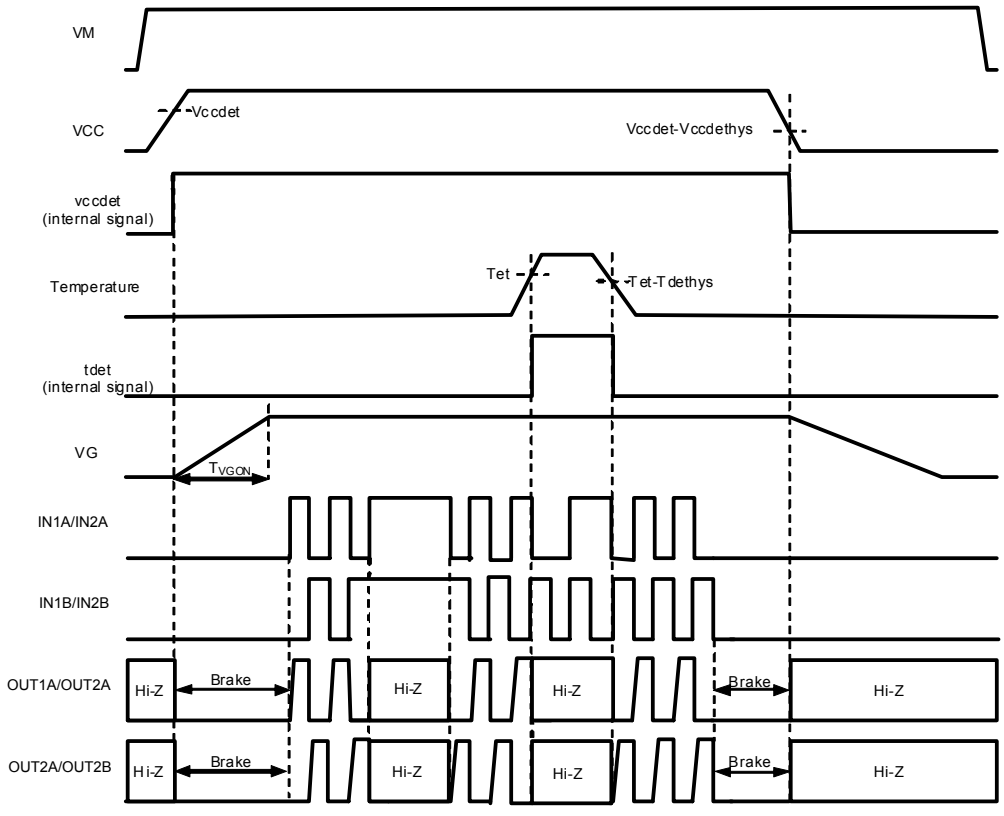


Figure 7. Timing chart of input and output signal (Tdet case)

FUNCTIONAL DESCRIPTION

FUNCTIONAL PIN DESCRIPTION

LOGIC SUPPLY (VCC)

The VCC terminal carries the logic supply voltage and current into the logic sections of the IC. VCC has an under-voltage threshold. If the supply voltage drops below the under-voltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input terminals control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are HIGH, the output bridges are both tri-stated (refer to **Table 4**, Truth Table).

H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These terminals provide connection to the outputs of each of the internal H-Bridges (See Figure 2, 34933 Simplified Internal Block Diagram).

MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output terminals. All VM terminals must be connected together on the Printed Circuit Board (PCB).

CHARGE PUMP (CL AND CH)

These two terminals, the CL and CH, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

POWER GROUND (PGND)

Power ground terminals must be tied together on the PCB and connected to the common ground plane.

LOGIC GROUND (EXPOSED PAD)

The Exposed Pad is connected to the PCB Ground plane through vias by soldering. Note the primary purpose of the Exposed pad for 34933 is thermal heat dissipation. Therefore, adequate thermal vias should be included in the PCB design. The exposed pad should be connected to the common ground plane.

VOLTAGE DETECTION AND THERMAL LIMIT DETECTION

The 34933 has the VCC Low Voltage Detection (Vccdet) and the Thermal Detection (Tdet). VCC Low Voltage Detection is designed to shutdown of IC functions when VCC becomes lower than specified voltage. Thermal Detection operates when the IC temperature exceeds specified value and stop H-Bridge operation. **Table 5** shows block status of 34933 by each condition. VCC is the control logic power supply for 34933. The system begins to operate when VCC > Vccdet (Typ. 2.2 V).

Table 5. Block Status

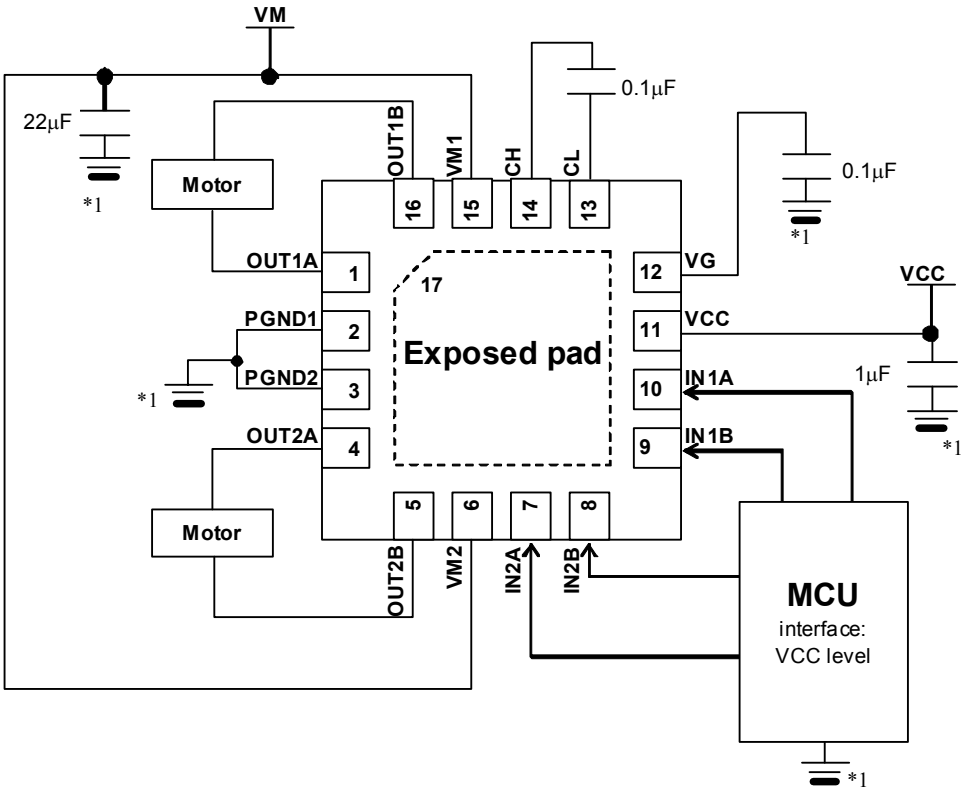
Operation mode	Vccdet	Tdet	Charge Pump	H-Bridge Driver
1	L	X	Disable	Disable
2	H	L	Enable	Enable
3	H	H	Enable	Disable

H - High
L - Low
X - Don't Care

TYPICAL APPLICATION

Figure 8 shows a typical application using the 34933. The internal charge pump of this device is powered from the VCC supply. Therefore, care must be taken to ensure VCC is a high enough value to provide sufficient gate-source voltage for the high-side MOSFETs when VM > VCC (e.g., VM = 5.0 V, VCC = 3.0\ V), in order to ensure full enhancement of the high-side MOSFET channels.

The 34933 can be configured in several applications. The figure below shows the 34933 in a typical Slave Node Application.



*1 - It is recommend to use low resistance copper PCB traces between VM & VCC ground and the PGND1/PGND2 pins.

Figure 8. Typical Application

PCB LAYOUT

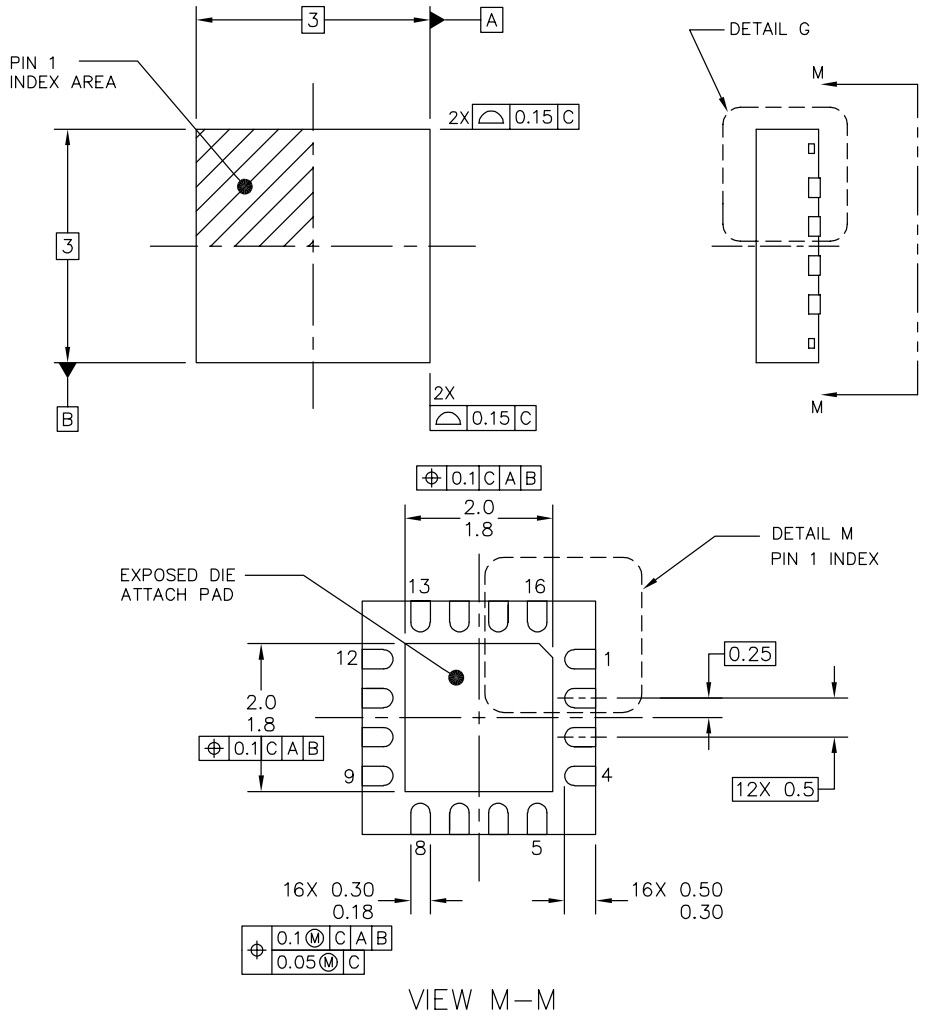
When designing a printed circuit board (PCB), connect sufficient capacitance between power supplies (VM & VCC) and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and the shortest possible distances. Note, capacitors should be placed as close to the 34933 as possible to maximize the filtering capability of each capacitor.

Additionally, care must be taken to avoid CEMF spikes induced when inductive currents accumulate at the VM supply. The typical method of snubbing inductive spikes includes connecting a Zener diode or capacitor at the supply terminal (VM).

PACKAGING

PACKAGE DIMENSIONS

Important: The package information is shown below. For the latest revision, please visit www.Freescale.com.



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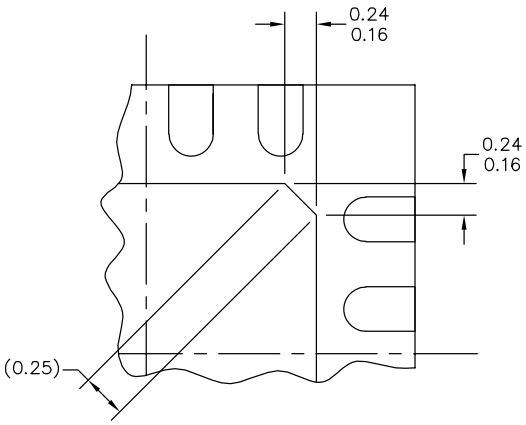
	CASE NUMBER: 2096–01	31 JUL 2009
	STANDARD: NON–JEDEC	

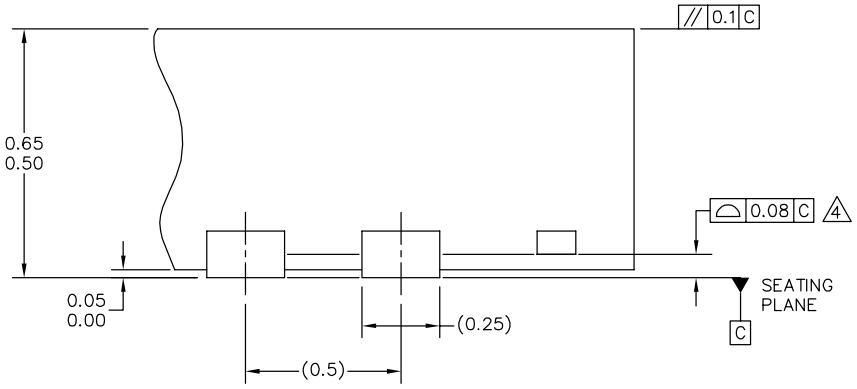
EP SUFFIX (PB-FREE)
16-PIN UQFN
98ASA00110D
REVISION O

34933

PACKAGE DIMENSIONS (Continued)



DETAIL M
PIN 1 BACKSIDE IDENTIFIER



DETAIL G
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	CASE NUMBER: 2096–01	31 JUL 2009
	STANDARD: NON–JEDEC	

EP SUFFIX (PB-FREE)
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98ASA00110D
REVISION O

34933

PACKAGE DIMENSIONS (Continued)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
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	STANDARD: NON–JEDEC	

EP SUFFIX (PB-FREE)
16-PIN UQFN
98ASA00110D
REVISION O

34933

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
2.0	7/2010	• Initial Release.

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